Integrator with p-channel depletion MOS switch

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***Abstract*—Current input, voltage output analog integrators are important electronic components for photo-current measurement applications such as diffuse light tomography and spectroscopy applications. In this work, current input, analog voltage output integrator has been designed and simulations have been tested for biomedical imaging purpose. Researchers want to know photon accumulations in different phantom layers for photon measurement applications, especially for diffuse optical tomography (DOT) devices. In continuous wave (CW) DOT (CWDOT) measurements, there is no way to guess photon trajectories except running Monte Carlo (MC) simulations on computer. In time resolved (TR) biomedical optic imaging systems there are some ways to guess photon trajectories, but this modality is requiring very expensive laboratory situations such as dark room, optical table, photo-multiplier tubes (PMT), scientific camera systems, etc. In this work, one analog integrator circuit has been designed to use for CWDOT systems in the future. Electronic current measurement sensor will be one pn type semiconductor photo-detector. Photo-detector current is modelled by current-source in simulations. The circuit is one integrator at top. Integrator has one operational amplifier, integrating capacitance, and switching n-channel and p-channel metal-oxide silicon (MOS) field-effect transistors (MOSFET). The purpose of this work is to accomplish to acquire different depth layer photons by the pn-type photo-detector from tissue or tissue phantom. To acquire different depth layer photons, time difference circuit should be designed. Time differences between different acquisitions are important parameter to guess penetration depth of photon accumulations. Time difference will be done by drawing layout of time delay circuit, but not in this work. One micrometer conducting length difference is generating approximately five femtoseconds time delay in average CMOS technology for polysilisium and metal wires. One n-channel MOSFET transistor switch and one low-voltage threshold inverse connected depletion mode p-channel MOSFET transistor are connected cascade to photodetector for time delay purpose. Integrating pulse signals are triggering switching transistors over delay line wires.**

Keywords—Analog integrator; p-channel depletion MOS switch

I. INTRODUCTION

In this work, one of the basic analog integrator topology has been used and simulation results have been illustrated with output waveform graphics. In general, analog integrators are integrating analog current input to voltage output. Pn-junction semiconductor photodetectors are connected forward-bias to analog integrator blocks. Analog integrator has the operational amplifier which has feedback capacitance from output to inversing or non-inversing input of operational amplifier. Usually integrator drawings are so simple, there is one basic operational amplifier and one feedback capacitance. From the view of application field, analog integrators can be designed in different ways. In the field of near infrared spectroscopy or diffuse light tomography for biomedical imaging purposes, photons can be collected under three major imaging modalities. These are continuous wave (CW), time resolved (TR), and frequency domain (FD) modulation techniques [1-3]. For these modalities, near infrared (IR) laser light is sent through imaging tissue or tissue like phantoms from one pencil beam source position. Regardless of any tissue type, from the different distance detector positions, migrated and diffused back reflected photons are collected by photo-detectors. Photo-detectors can be pn-type junction semiconductor photodiodes, scientific cameras, or photo-multiplier tubes (PMT). In generally, pn-type semiconductor photodetectors are used for CW diffuse light imaging modality [4-6]. Photodiode photodetectors usually have very effective active area. They are very high-speed detectors. Optoelectronic companies are also trying to achieve fully depleted working mode. They have very fast light response time; hence they have small low junction capacitances. They can achieve faster response times such as in pico-seconds. These detectors can work in ultra-dark room conditions, they can collect small number of photons. In this work, it is presumed that one of this semiconductor photodetector [7] is connected to our analog integrator block in forward biased current flow mode. From the view of diffuse optical tomography (DOT) biomedical imaging field, it might be good to categorize back-reflected collected photons as they are coming from different depth layers. Depth information is important for the optic tomography researchers. Diffuse light penetration depth is the key element to build photon trajectories which are generating photon weight function coefficients inside the tissue. If someone had a device which it could group different depth layer photon trajectories, this information would be used in CWDOT image reconstruction algorithms, helpfully. If analog integrator could be run in very short time

difference mode, photons which are collected from different depth layers would be grouped successfully. For this purpose, some very complicated digital-to-time converters (DTC) can be used [8] to switch analog integrator capacitance in different time periods. But using DTC method can be time consuming, and expensive from the view of ASIC (Application specific integrated circuit designer) companies and there is also high amount of production cost. In this work, instead of using DTC techniques or some other complicated switching capacitance circuit topologies, one simple analog integrator [9,10], with p-channel depletion mode metal-oxide silicon (MOS) field-effect transistor (MOSFET) switch has been used. The circuit topology has one integrator and MOS transistors as switches. Phases have been modelled by delay phase pulses.

II. METHOD

The analog integrator has been designed and schematic drawing simulations have been run with spice model parameters for educational product design kit (PDK). The analog integrator has basic differential amplifier stage which has 2 n-channel, and 2 p-channel MOSFET transistors. Analog integrator has one feed-back capacitance between output and input of operational amplifier. In Fig.1 schematic drawing of circuit topology can be seen.

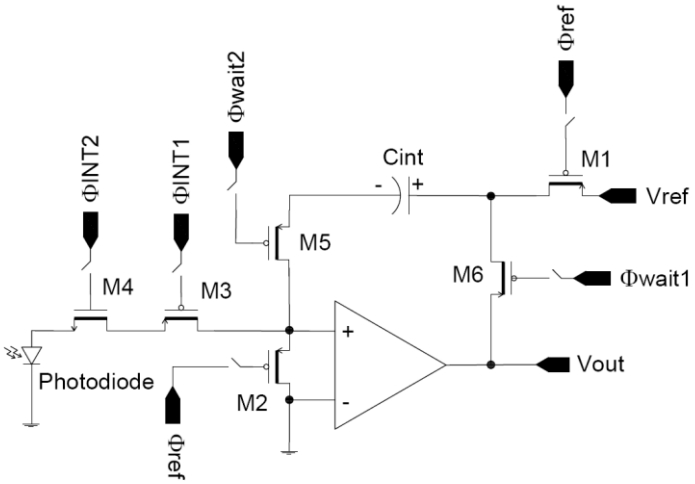


Fig. 1. Analog integrator topology

According to the proposed circuit topology model, phase differences have been modelled by integrating pulse inputs ΦINT1 and ΦINT2 signals. These pulse inputs are triggering M3 and M4 MOS transistors. M3 is the inverse connected p-channel low voltage threshold depletion mode MOSFET transistor. M4 is the regular forward-bias connected n-channel MOS transistor. According to the proposed circuit model, if integrating ΦINT1 and ΦINT2 pulses trigger in exactly the equal time, photodiode current does not flow, hence normally-closed (NC) M3 depletion mode p-channel MOSFET transistor switch will cut-off immediately. On the other hand, if any time differences occur between two integrating pulses, at the beginning of run, normally open (NO) n-channel M4 MOSFET transistor will turn ON. M3 p-channel MOSFET transistor will be ON now, because it is normally closed (NC) switch. When lagging ΦINT1 pulse signal arrives triggering gate input of M3 p-channel MOSFET transistor, M3 switch will open the circuit. Cint integrating capacitance will integrate input photodiode current in this time. In this work, time delay has been modelled by phase differences by ΦINT1 and ΦINT2 pulses between M3 and M4 switching transistors. In real layout process, time delay will be made by wire length differences of metal or polysilicon gate triggering line, in the future. Each one micrometer conducting length difference is generating approximately 5 femtoseconds time delay [11].

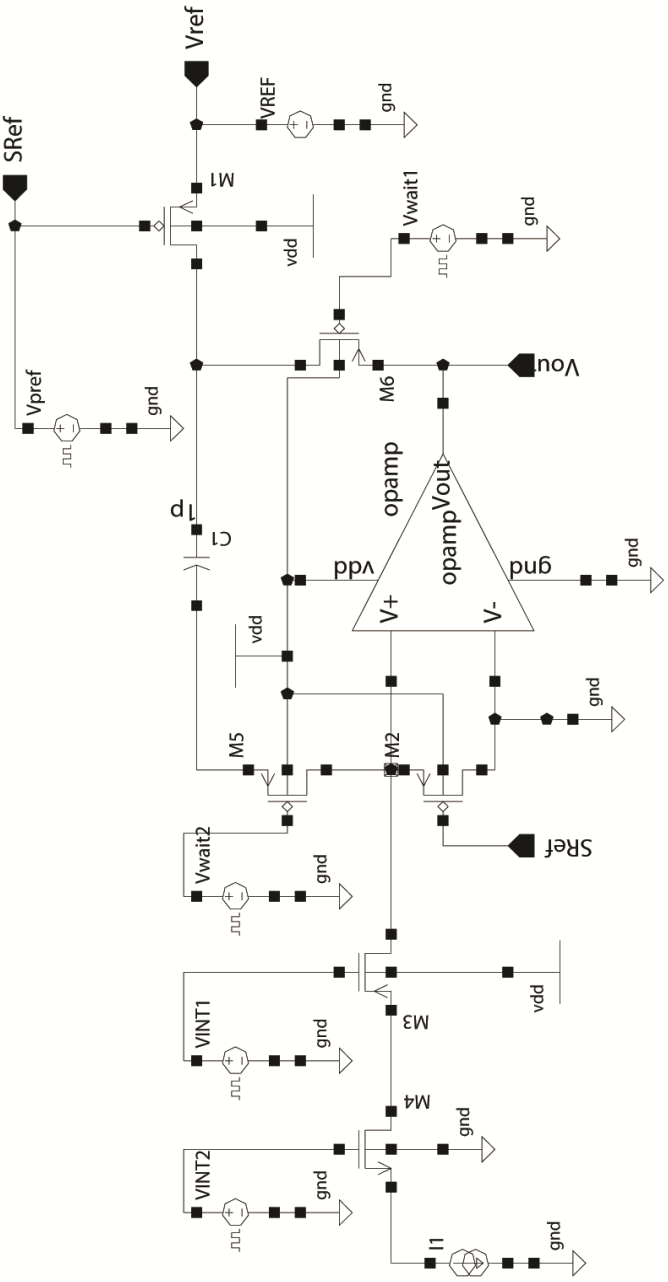


Fig. 2. Analog integrator without transistor switching noise suppression

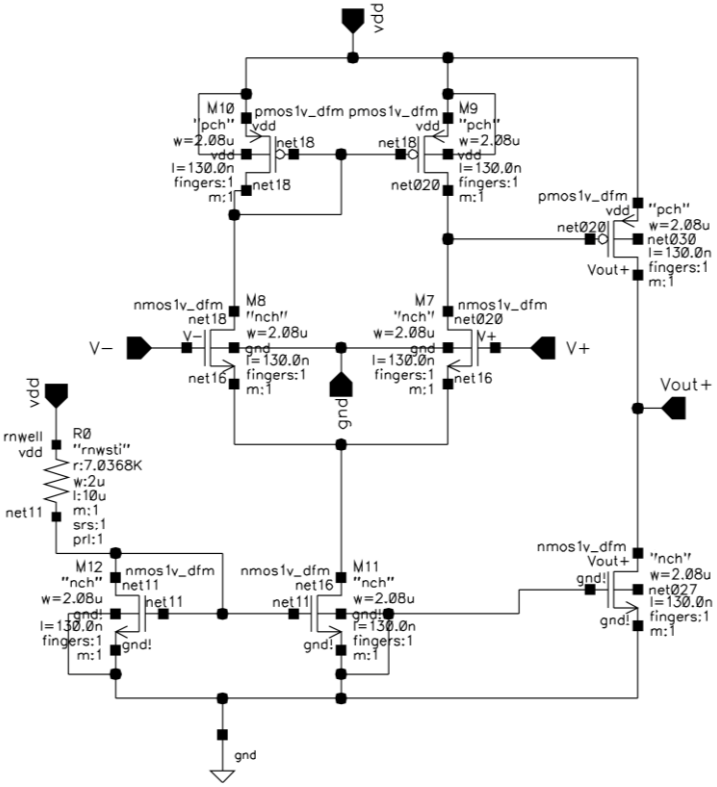


Fig. 3. Operational amplifier

The circuit has twelve MOSFET transistors, five of them are n-channel and the other seven are p-channel. Integrator has one basic operational amplifier stage at the core. MOSFET transistors in Fig.2 are switching transistors. Operational amplifier circuit has one differential amplifier as it can be seen in Fig. 3. Transistors M1, and M2 are supplying 1 vdc reference Vref voltage to analog integrator circuit. Transistors M5, and M6 are isolating C1 integrator capacitance from circuit, by this way holding reference voltage over C1 capacitance. Transistors M3, and M4 are integrating switch transistors. M4 is n-channel, M3 is inverse connected p-channel depletion-mode MOSFET transistor. M3 and M4 transistors' gate triggering input pulses are VINT1, and VINT2. VINT1 has -1 volt to 0 pulse voltage which has 1 microsecond pulse duration and 10 microsecond time periods. VINT2 has 0 to 1-volt pulse voltage which has 1 microsecond pulse duration and 10 microsecond time periods. At the beginning of circuit design, it is thought that time delay differences will be generated between M3 and M4 transistors' triggering gate nodes by using delay wire lines. When transistor M4 is turned ON, transistor M3 will still be ON now, hence p-channel inverse-biased depletion mode MOSFET is normally ON. In circuit simulation, this time delay difference has been modelled by delay parameter. In real world, when the design continues in layout level, the time delay will be made by triggering gate wire length differences. 20 µm length difference is making 100 femtoseconds time delay between two lines. When integrating switch transistor M4 is ON, after some time delay normally closed (NC) M3 integrating switch transistor is turning OFF. In this delta time, analog integrator is integrating input photo-detector current. In this circuit, photo-current has been modelled by 1 pico-ampere (pA). Integrating capacitance has been selected as 1 pico-farad (pF).

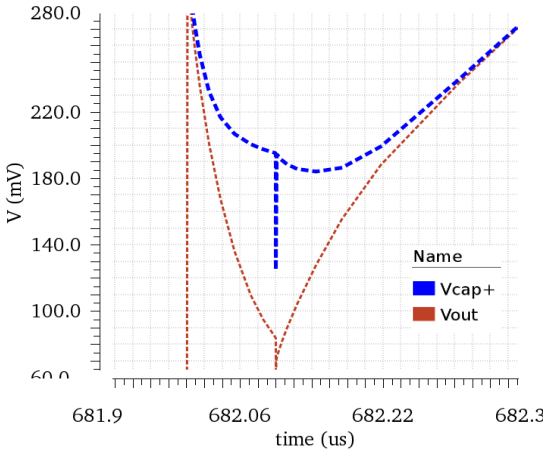


Fig. 4. One microsecond integration time Vcap+, Vout voltages

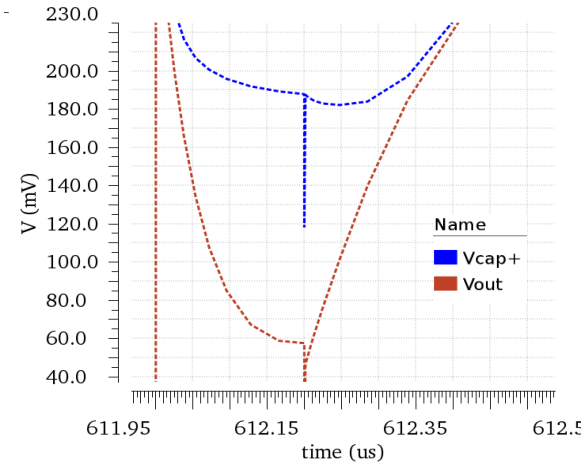


Fig. 5. Two microsecond integration time Vcap+, Vout voltages

Output voltage levels and simulation signals can be seen in Fig. 4, Fig. 5, and Fig. 6, respectively. In Fig. 4, one microsecond integration time Vout voltage level is 75 mV, in Fig. 5, two microseconds integration time, it is dropping to almost 55 mV. In Fig. 6, dashed red line is showing Vout output integrator voltage. Vout output voltage has integrating shape. The other signals, blue and brown are Vwait1 and Vwait2 pulse signals which are opening integrating capacitance' connection nodes, hence holding voltage over capacitance, pink is Sref, orange and green are VINT1, and VINT2, magenta is Vcap+. Transistor channel lengths have been selected as 130 nm, transistor channel widths have been selected as w=2.08 um. According to Eq.1, 6 Ghz cutoff frequency low pass RC filters have been applied to gate terminal input of switching transistors. R=10 kohm, and C=100

fF capacitance values have been selected. The new circuit is illustrated in Fig. 7. In Fig. 8, and Fig. 9 the effect of RC low pass filters can be seen, hence there is no notch at switching time.

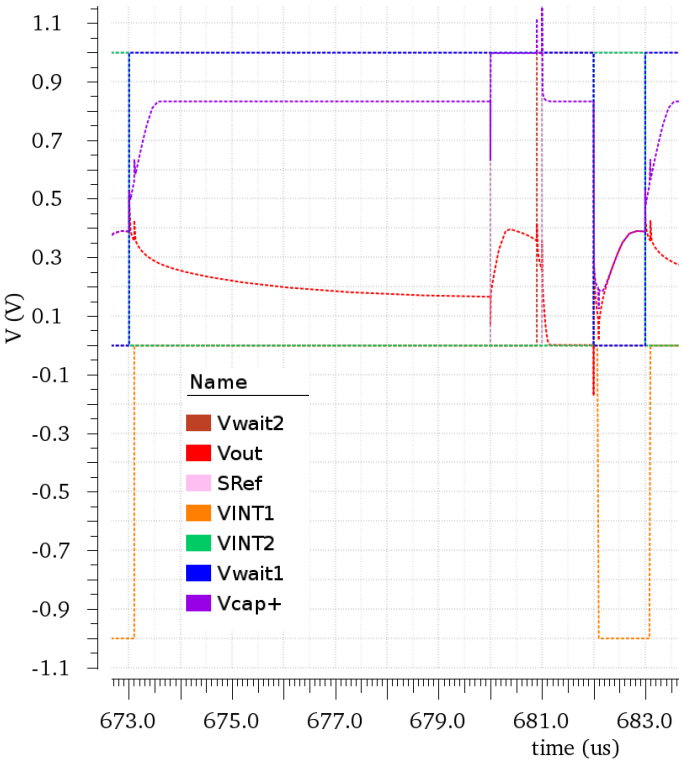


Fig. 6. Time vs. signals

There is also integral nonlinearity (INL) which starts at 2 microsecond integration time which can be seen in Fig. 5 and Fig. 9. These graphics have also transistor switching noise notches which can be seen from pictures. To be able to eliminate these noises, analog integrator has been modified as in Fig. 7. Low-pass RC filters have been added into transistor gate inputs.

$$f_c = \frac{1}{2\pi RC} \qquad (1)$$

III. CONCLUSION

In this work, presumed simulation results have been seen according to proposed circuit model. This work comprises only proposed circuit topology model and simulation results. Circuit layout will be drawn, and post-simulations will be run in the future. Microelectronic integrated circuit (IC) will be realized. The main idea of this work was to show new analog integrator circuit which is using the time delay advantage of delay lines and delayed activation of inverse connected depletion mode p-channel MOSFET transistor. In the simulations, delay line has been modelled as delay pulse signals. Simulation results have illustrated us that delay line circuit can be used to acquire different depth layer photons from tissue or tissue-like phantoms by using novel analog integrator and photodiode.

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I designed and simulated circuit in the Akdeniz University Faculty of Engineering, Department of Biomedical Engineering, Mechanical Engineering corridor, room number B304, Konyaalti, ANTALYA, TURKEY.

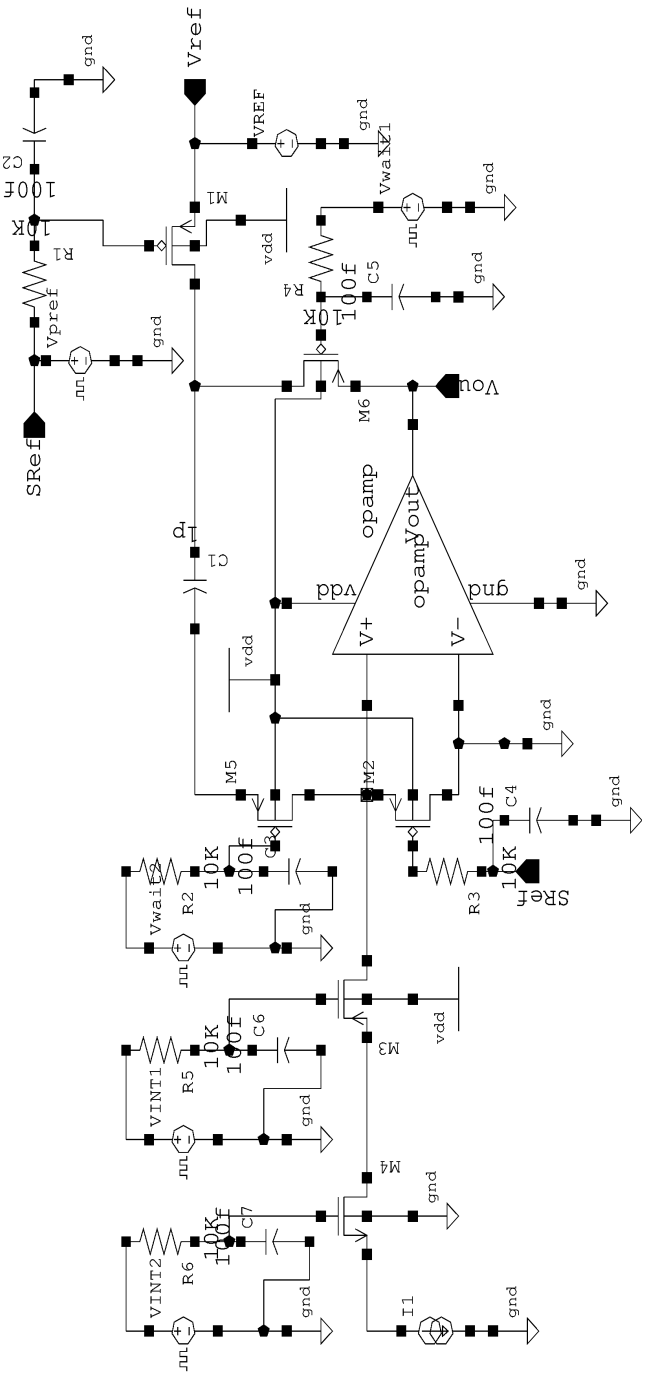


Fig. 7. Analog integrator with transistor switching noise suppression

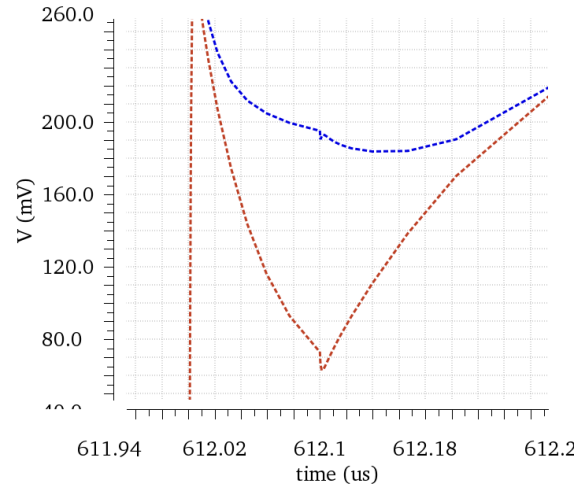


Fig. 8. One microsecond integration time Vcap+, Vout voltages with low-pass filter

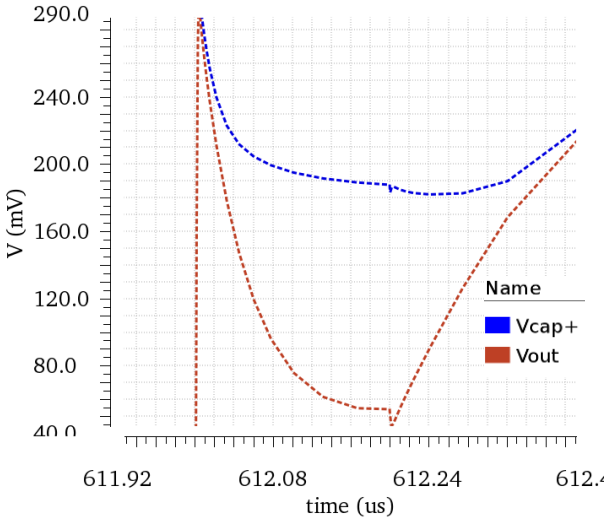


Fig. 9. Two microseconds integration time Vcap+, Vout output voltage with low-pass filter

References

[1] D.A. Boas, D.H. Brooks, E.L. Miller, C.A. DiMarzio, M. Kilmer, R.J. Gaudette, Q. Zhang, "Imaging the body with diffuse optical tomography," IEEE Signal Processing Magazine, vol. 18, no. 6 pp. 55-75, November 2001.

[2] X. Intes, B. Chance, "Multi-frequency diffuse optical tomography," Journal of Modern Optics, 52:15, 2139-2159, 2005.

[3] A.P. Gibson, J.C. Hebden, S.R. Arridge, "Recent advances in diffuse optical imaging," Phys. Med. Biol., 21;50(4):R1-43, February 2005.

[4] A.H. Hielscher, A.Y. Bluestone, G.S. Abdoulaev, A.D. Klose, J. Lasker, M. Stewart, U. Netz and J. Beuthan, "Near-infrared diffuse optical tomography," Disease Markers, vol. 18, pp. 313-337, 2002.

[5] A. Siegel, J.J. Marota, D. Boas, "Design and evaluation of a continuous-wave diffuse optical tomography system," Opt. Express. 12;4(8):287-98. April 1999.

[6] X. Cheng, D.A. Boas, "Diffuse optical reflection tomography with continuous-wave illumination," vol. 3, no. 3, pp. 118-123, 1998.

[7] OSI optoelectronics OSD35-lr-d photovoltaic mode, UV enhanced series photodiode.

[8] J. Z. Ru, C. Palattella, P. Geraedts, E. Klumperink, and B. Nauta, "A High-Linearity Digital-to-Time Converter Technique: Constant-Slope Charging," IEEE journal of solid-state circuits, vol. 50, no. 6 pp. 1412-1423, June 2015.

[9] P. R. Gray, P. J. Hurst, S. H. Lewis, and R.G. Meyer, Analysis and Design of Analog Integrated Circuits, 5th ed. Wiley, March 2001.

[10] DDC232 datasheet manual. Burr-Brown, TX, April 2010.

[11] IPC Association Connecting Electronics Industries, IPC-TM-650 test methods.