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New highly linear tunable transconductor circuits with low number of MOS transistors

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ABSTRACT

In this article, two new highly linear tunable transconductor circuits are proposed. The transconductors employ only six MOS transistors operated in saturation region. The second transconductor is derived from the first one with a slight modification. Transconductance of both transconductors can be tuned by a control voltage. Both of the transconductors do not need any additional bias voltages and currents. Another important feature of the transconductors is their high input and output impedances for cascadability with other circuits. Besides, total harmonic distortions are less than 1.5% for both transconductors. A positive lossless grounded inductor simulator with a grounded capacitor is given as an application example of the transconductors. Simulation and experimental test results are included to show effectiveness of the proposed circuits.

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KEYWORDS
MOSFET circuits; transconductor; inductor simulator

1. Introduction

Transconductors are the basic building blocks in many analogue circuits such as continuous-time filters. They convert specific range of input voltages to output currents with a transconductance factor (G_m). There are different techniques to perform linear transconductors. Some linear transconductors have been proposed with triode-mode transistors (Fayed & Ismail, 2005; Gatti, Maloberti, Palmisano, & Torelli, 1994). The transconductor circuit in Fayed and Ismail (2005) uses two operational amplifiers (OAs). The configuration in Gatti et al. (1994) has two bias current sources; thus, it needs extra circuitry. Another approach for linearization of transconductors is source-degeneration technique (Kuo & Leuciuc, 2001; Martinez-Heredia & Torralba, 2011; Worapished & Naphaphan, 2003). A resistor is used between differential pairs for resistive source-degeneration in Worapished and Naphaphan (2003) and the degeneration resistor is implemented by using MOS transistors in Kuo and Leuciuc (2001). An enhanced source-degenerated transconductor circuit in Martinez-Heredia and Torralba (2011) utilizes super-transistor circuits. Nevertheless, it contains a great number of transistors. Also, the configurations in Worapished and Naphaphan (2003), Kuo and Leuciuc (2001) and Martinez-Heredia and Torralba (2011) include one or more bias sources. A fully differential difference transconductor (FDDT) configuration in Mahmoud and Soliman (1999) is based on the use of matched MOS transistors in the saturation region, but this configuration has a large number of transistors. A transconductor configuration with local feedback in Ohbuchi and Matsumoto (2013) uses MOS transistors in the subthreshold region to reduce nonlinear effects. However, it requires extra circuitry to obtain the output current. Another MOS transconductor in Tongpoon, Matsumoto, Takeuchi, Ohbuchi, and Ishio (2012) with local feedback is configured for cancellation of

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mobility degradation problem. But, this configuration has both a floating control current source and a bias voltage. The transconductor circuit in Vlassis and Raikos (2012) with three bias sources has been proposed using master–slave technique. Additionally, an adjustable transconductor application in Vlassis and Raikos (2012) needs four OAs. The transconductor circuit in Torralba, Martìnez-Heredia, Carvajal, and Ramìrez-Angulo (2002), which consists of supercascode transistors for linearization, requires extra circuitry. The linearized transconductor in Ismail and Soliman (2000) with long-tail differential pairs includes a large number of transistors and nonlinear terms in the output current equation. MOS transistors in triode region have been used to achieve a transconductor such as the configuration in Han (2006). However, this circuit has a large number of transistors. Bias offset voltage technique is implemented in the configuration of Yamaguchi, Matsumoto, and Noguchi (2005), but its drawback is the requirement of four bias voltage sources. Some transconductors are designed with class-AB (Demosthenous & Panovic, 2005; El-Adawy & Soliman, 2000). Nevertheless, the circuit in Demosthenous and Panovic (2005) needs extra circuitry to obtain output current and employs a large number of transistors. Also, two bias voltages and two control current sources are required to realize the configuration in El-Adawy and Soliman (2000). The MOS transistor-based transconductor element in Nauta (1992) has differential-pair structure. But, it does not have the property of tunability and needs extra circuitry to obtain output current. The transconductor of Krummenacher, Vittoz, and Degrauwe (1981) uses only two MOS transistors, but it does not have the feature of tunability. The transconductor of Park and Schaumann (1986) employs only four MOS transistors, whereas it requires two symmetrical control voltages. A complete circuit of the transconductor of Nedungadi and Viswanathan (1984) consists of two control currents; thus, it needs two extra MOS transistors. Also, it is well-known that a simple operational transconductance amplifier-based transconductor employs only five MOS transistors; however, it operates in small signals. On the other hand, there are a number of grounded inductor simulators in related literature (Gift, 2004; Maundy & Gift, 2011; Metin, 2012; Yuce, 2007, 2009).

This article proposes two new highly linear tunable transconductor configurations. Both of the transconductors include only six MOS transistors in the saturation region. They do not need extra bias current or voltage sources. The transconductance can be linearly tuned by a control voltage. An advantage of the proposed transconductors is their high input and output impedances. As an application, a positive lossless grounded inductor simulator using two proposed transconductors is implemented. Simulation and experimental test results are included to demonstrate the performance and workability.

The article is organized as follows: After introduction is given in Section 1, a transconductor is described and the proposed transconductor structures are treated in Section 2. Inductor simulator application is given in Section 3. Simulation and experimental test results for the proposed circuits are given in Section 4. Finally, some conclusion remarks are drawn in Section 5.

2. Proposed linear tunable transconductor

A tunable transconductor has three terminals which are input voltage (V_{in}), output current (I_{out}) and control voltage (V_C). Electrical symbol of the tunable transconductor is shown in Figure 1. G_m in Figure 1 is defined by the following equation:

$$G_m = \frac{I_{out}}{V_{in}} \tag{1}$$

A common-source (CS) stage with diode-connected load (Minaei & Yuce, 2012; Razavi, 2008) in Figure 2 is used in the proposed transconductor. If the channel length modulation effect is not taken into account and $V_{in} \leq V_{TNa}/2$, the input/output characteristics of the CS stage can be given as

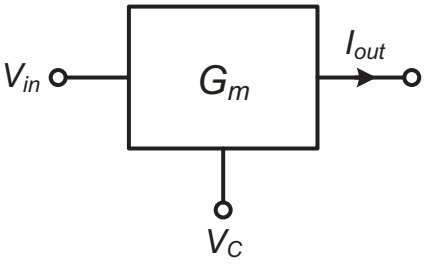

Figure 1. Electrical symbol of the tunable transconductor.

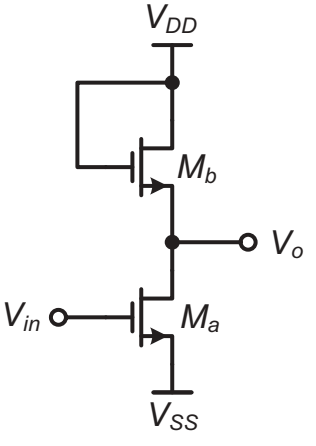

Figure 2. Simple CS stage with diode-connected load (Minaei & Yuce, 2012; Razavi, 2008).

$$V_o = V_{DD} - V_{TNb} + \sqrt{\frac{k_{na}}{k_{nb}}}(V_{SS} + V_{TNa}) - \sqrt{\frac{k_{na}}{k_{nb}}}V_{in} \tag{2}$$

In (2), $V_{TNa} = V_{TN0}$ and V_{TNb} is found as

$$V_{TNb} = V_{TN0} + \gamma\left(\sqrt{2\phi_F + V_o - V_{SS}} - \sqrt{2\phi_F}\right) \tag{3}$$

where V_{TN0} is threshold voltage of the NMOS transistor without body effect, $k_n = \mu_n C_{ox}$ *(W/L)* is the transconductance parameter of the NMOS transistor, μ_n is the mobility of the carrier for NMOS transistor, C_{ox} is the gate oxide capacitance per unit area, W is the channel width, L is the channel length and ϕ_F is the Fermi voltage. Also, it is seen from (3) that V_{TNb} has a non-linear term. If $V_o \lll 2\phi_F - V_{SS}$, (3) approximately turns to

$$V_{TNb} \cong V_{TN0} + \gamma\left(\sqrt{2\phi_F - V_{SS}} - \sqrt{2\phi_F}\right) \tag{4}$$

If channel length modulation effects for the circuit in Figure 2 are considered, the circuit of Figure 2 has non-linear terms which can be reduced by increasing channel lengths of the NMOS transistors (Razavi, 2008).

If it is assumed that $V_{TNa} = V_{TNb}$ and $k_{na} = k_{nb}$, the output voltage of the CS stage can be written as

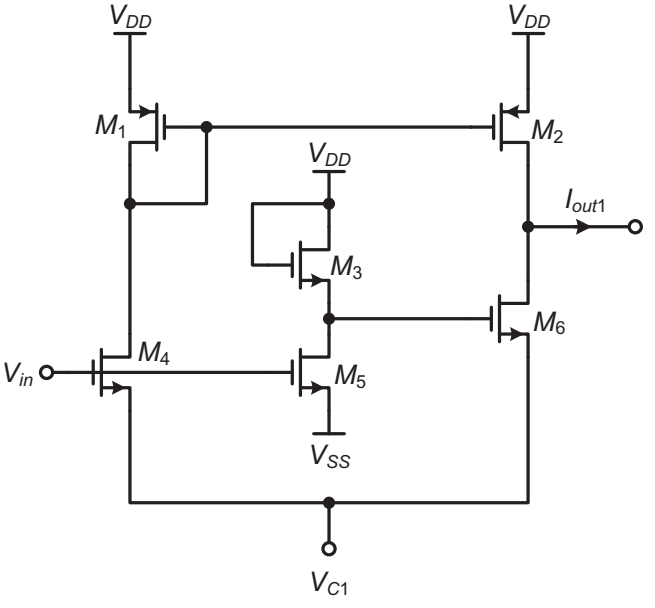

Figure 3. The first proposed transconductor configuration.

$$V_o = -V_{in} \tag{5}$$

A simple unity gain inverting amplifier is obtained from Equation (5) (Minaei & Yuce, 2012; Razavi, 2008). It is used for cancelling squared terms in the expressions of the proposed transconductors.

The first proposed transconductor configuration is given in Figure 3. It consists of only six MOS transistors, M_1–M_6, and a control voltage, V_{C1}. In this circuit, all the bulks of the MOS transistors are connected to the corresponding sources to ignore the body effects. M_1 and M_2 transistors are used for realizing a current mirror. M_3 and M_5 transistors constitute a simple unity gain inverting amplifier where the transconductance parameters of the transistors M_3 and M_5 are equal, $k_{n3} = k_{n5}$(Minaei & Yuce, 2012; Razavi, 2008). Additionally, V_{DD} and V_{SS} respectively refer to positive and negative supply voltage sources and V_{SS} equals to $-V_{DD}$. It is assumed that all the MOS transistors in Figure 3 operated in the saturation region ($V_{GS} > V_{TN}$ and $V_{DS} > V_{GS} - V_{TN}$ for NMOS transistors, $V_{SG} > \left|V_{TP}\right|$ and $V_{SD} > V_{SG} - \left|V_{TP}\right|$ for PMOS transistors). Here, V_{TN} and V_{TP} are the threshold voltage of the NMOS and PMOS transistors, respectively. It is assumed that transconductance parameters of the transistors M_4 and M_6 are respectively equal to k_n and $\Delta k + k_n$. The drain currents of the transistors M_4 and M_6 in Figure 3 can be respectively given by the square-law relation as

$$I_{D4} = \frac{1}{2} k_n (V_{in} - V_{C1} - V_{TN})^2 \tag{6a}$$

$$I_{D6} = \frac{1}{2} (k_n + \Delta k)(-V_{in} - V_{C1} - V_{TN})^2 \tag{6b}$$

Here, if the body effect is considered, V_{TN} is evaluated as

$$V_{TN} = V_{TN0} + \gamma\left(\sqrt{2\phi_F + V_{C1} - V_{SS}} - \sqrt{2\phi_F}\right) \tag{7}$$

In Figure 3, I_{D2} is equal to I_{D4}. Also, I_{Dn} (n = 1, 2, …, 6) is the drain current flowing through corresponding MOS transistor. The output current I_{out1} is obtained by the subtraction of I_{D6} from I_{D2} as below

$$I_{out1} = I_{D2} - I_{D6} = -(2k_n + \Delta k)(V_{C1} + V_{TN})V_{in} - \frac{1}{2}\Delta k V_{in}^2 - \frac{1}{2}\Delta k(V_{C1} + V_{TN})^2 \tag{8}$$

If Δk is equal to zero, (8) converts to

$$I_{out1} = I_{D2} - I_{D6} = -2k_n(V_{C1} + V_{TN})V_{in} \tag{9}$$

Here, $V_{C1} < -|V_{in}| - V_{TN}$ condition should be satisfied for proper operation of the proposed transconductor. From (9), the transconductance G_{m1} of the first proposed circuit is found as

$$G_{m1} = -2k_n(V_{C1} + V_{TN}) \tag{10}$$

It is seen from (10) that G_{m1} has a linear characteristic. Also, the second proposed circuit shown in Figure 4 with $k_{n3} = k_{n5}$ is derived from first proposed circuit by slight modifications such that the output current in the first proposed transconductor is taken outside while the output current in the second proposed transconductor is taken inside. It is assumed that transconductance parameters of the transistors M_4 and M_6 are equal to k_n, and the drain currents of the transistors M_4 and M_6 in Figure 4 can be respectively given by the square-law relation as

$$I_{D4} = \frac{1}{2}k_n(V_{in} - V_{C2} - V_{TN})^2 \tag{11a}$$

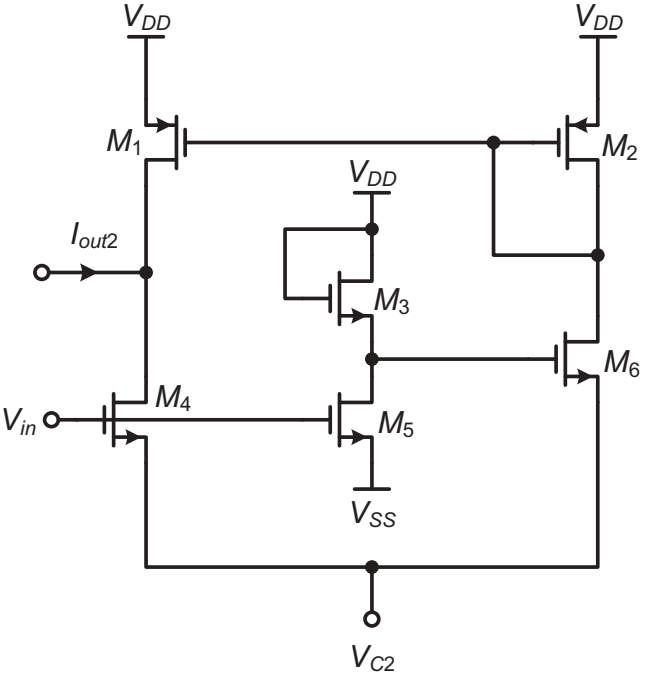

Figure 4. The second proposed transconductor configuration.

$$I_{D6} = \frac{1}{2}k_n(-V_{in} - V_{C2} - V_{TN})^2 \tag{11b}$$

I_{D1} is equal to I_{D6} in Figure 4. The output current I_{out2} is obtained by the subtraction of I_{D4} from I_{D1} as below:

$$I_{out2} = I_{D4} - I_{D1} = -2k_n(V_{C2} + V_{TN})V_{in} \tag{12}$$

Here, $V_{C2} < -|V_{in}| - V_{TN}$ condition should be satisfied for proper operation of the second proposed transconductor. Similarly, from (12), G_{m2} of the second proposed transconductor is obtained as follows:

$$G_{m2} = -2k_n(V_{C2} + V_{TN}) \tag{13}$$

Input impedances of the first and second proposed transconductors are ideally infinity. Output impedances of both transconductors are respectively evaluated as

$$R_{out1} = r_{o2} \,//\, r_{o6} \tag{14a}$$

$$R_{out2} = r_{o1} \,//\, r_{o4} \tag{14b}$$

Small signal model of the first proposed transconductor is given in Figure 5. Also, i_{out}/v_{in} in Figure 5 is approximately evaluated as follows:

$$\frac{i_{out}}{v_{in}} \cong \frac{g_{m5}g_{m6}}{g_{m3}} - \frac{g_{m2}g_{m4}}{g_{m1}} \tag{15}$$

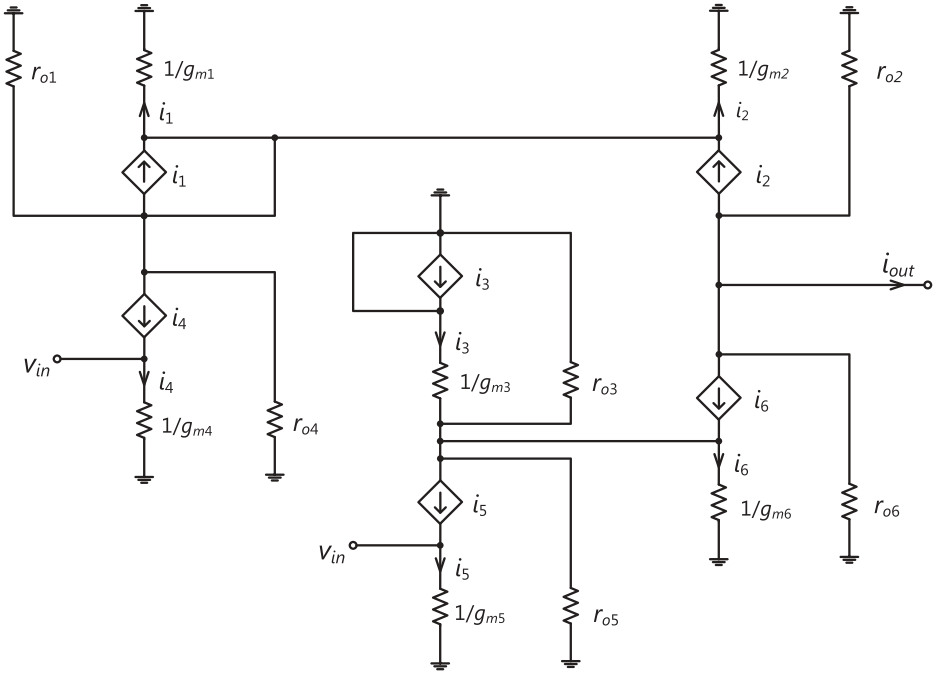

Figure 5. Small signal model of the first proposed transconductor.

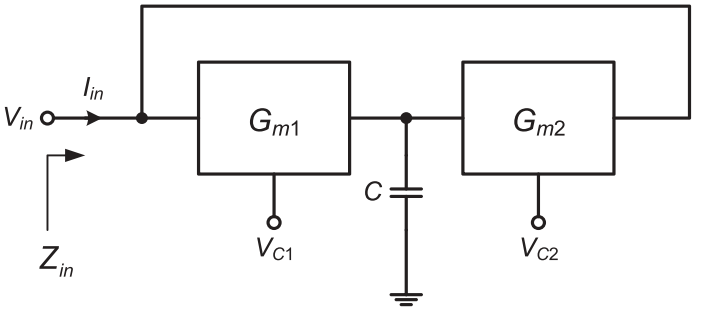

Figure 6. The proposed positive lossless grounded inductor simulator employing a grounded capacitor (Geiger & Sánchez-Sinencio, 1985).

3. An application example: inductor simulator

As an application example, a positive lossless grounded inductor simulator in Figure 6 can be implemented by using two transconductors (Geiger & Sánchez-Sinencio, 1985). While one of the used transconductors is the first proposed circuit in Figure 3, the other one is the second proposed circuit in Figure 4. V_{C1} and V_{C2} are control voltages. The input impedance of the proposed inductor simulator is obtained as

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{sC}{G_{m1}G_{m2}} \tag{16}$$

In order to obtain a negative lossless inductor simulator using a grounded capacitor, the first proposed transconductor is replaced instead of the second proposed transconductor in Figure 4 or vice versa.

4. Simulation and experimental test results

Simulation results are achieved by SPICE program using level 7 0.25 µm Taiwan Semiconductor Manufacturing Company, Ltd. (TSMC, Hsinchu, Taiwan, R.O.C.) CMOS technology parameters (Yuce, Minaei, & Cicekoglu, 2006). The symmetrical DC power supply voltages are selected as $V_{DD} = -V_{SS} = 1.25$ V. The aspect ratios (W/L) of the MOS transistors in the proposed circuits in Figures 3 and 4 are given in Table 1. As shown in Table 1, $M_1 - M_2$ (PMOS) and $M_3 - M_6$ (NMOS) transistors are matched to each other for a simplified design.

Figure 7 illustrates the output current of the first proposed transconductor with respect to input voltage where the control voltage is changed from −1.2 V to −0.6 V with a step size of 0.1 V. Here, $V_{in} < V_{TH}/2$ should be satisfied for proper operation condition ($V_{TH} \cong 0.38$ V for NMOS transistors and $V_{TH} \cong -0.57$ V for PMOS transistors) (Minaei & Yuce, 2012; Razavi, 2008; Yuce et al., 2006). Figure 8 illustrates G_m characteristics of the first proposed transconductor with respect to V_{C1}. As shown in Figure 8, it has good linearity. Figure 9 indicates the power consumption variations of the first proposed transconductor against V_{C1}. Power consumption of the proposed inductor simulator is found as 2.01 mW when control voltages are $V_{C1} = V_{C2} = -0.8$ V.

Table 1. Dimensions of the MOS transistors.

Transistor name	W/L
M_1, M_2	15 µm/1 µm
M_3, M_4, M_5, M_6	5 µm/1 µm

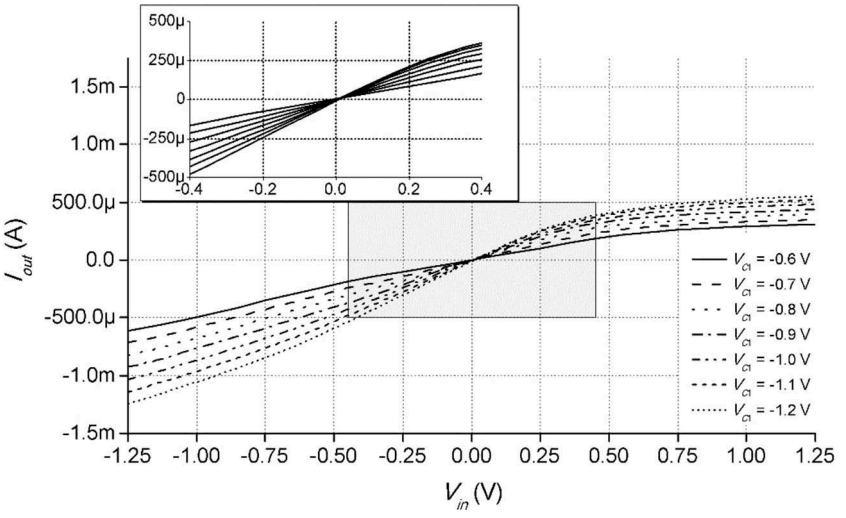

Figure 7. DC transfer characteristics of the first proposed transconductor.

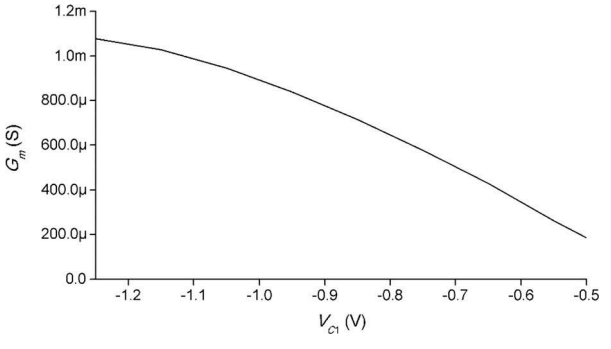

Figure 8. The variation of the transconductance G_m versus V_{C1}.

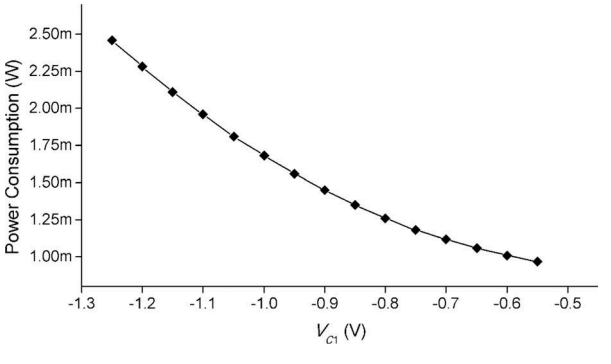

Figure 9. Power consumption versus V_{C1} of the first proposed transconductor.

The gain and phase responses of the first proposed transconductor are shown in Figure 10 where V_{C1} = −0.8 V is chosen. It is seen from Figure 10 that cut-off frequency of the first proposed transconductor is about 440 MHz. Therefore, the first proposed transconductor can

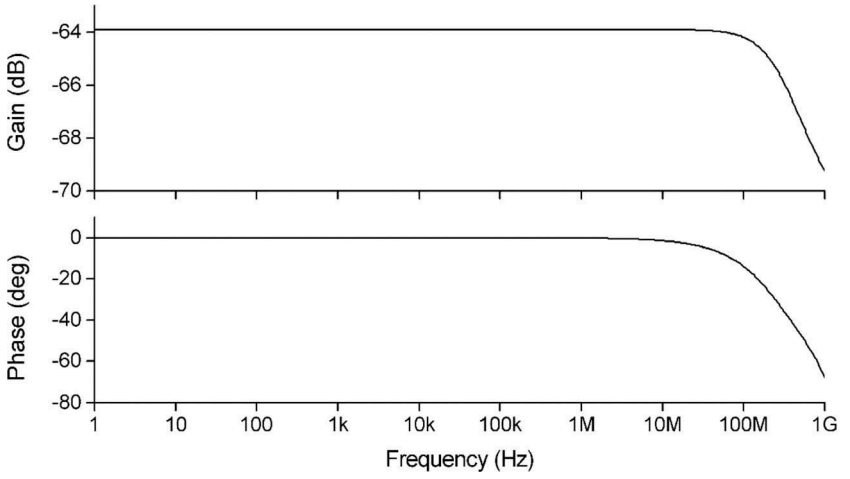

Figure 10. Frequency characteristics of the first proposed transconductor.

be operated at about 44 MHz (Yuce & Minaei, 2008). A sinusoidal voltage signal with 100 mV peak value at 10 MHz is applied to the input of the first proposed transconductor circuit where $V_{C1} = -0.8$ V is chosen. The sinusoidal input voltage and the corresponding output current signals are depicted in Figure 11. As an example, only the channel widths of M_3 – M_6 transistors of the first proposed transconductor are varied between 4 μm and 6 μm with a step size of 0.25 μm where $V_{C1} = -0.8$ V is chosen. The input and corresponding output responses are drawn in Figure 12 in which the circuit is not much affected by variations of the MOS transistor dimensions. A 1 kΩ load resistor is connected to output terminal of the first proposed transconductor where $V_{C1} = -0.8$ V is chosen. The input and output noise variations against frequency are shown in Figure 13, which are adequately low values. The total harmonic distortion (THD) variations with respect to peak values of the applied sinusoidal signal at the frequency of 10 MHz are depicted in Figure 14 where a 1 kΩ load resistor is connected to the output for V_{C1} is −0.6 V, −0.8 V and −1 V. It is seen from Figure 14 that THD variations are smaller than 1.5%.

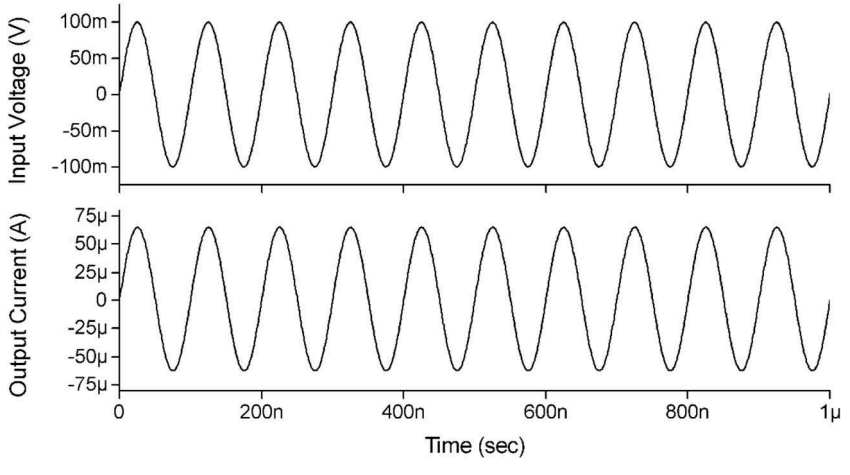

Figure 11. Transient analysis of the first proposed transconductor.

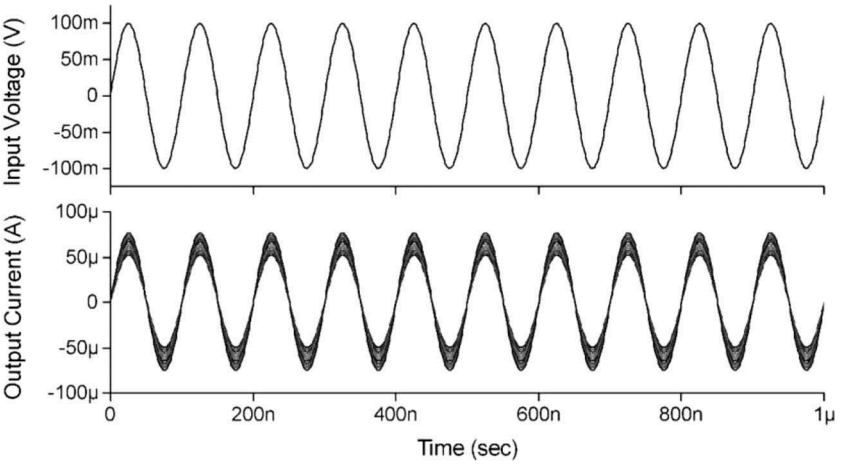

Figure 12. Time-domain response for the variation of width (W) parameter of the MOS transistors M_3–M_6.

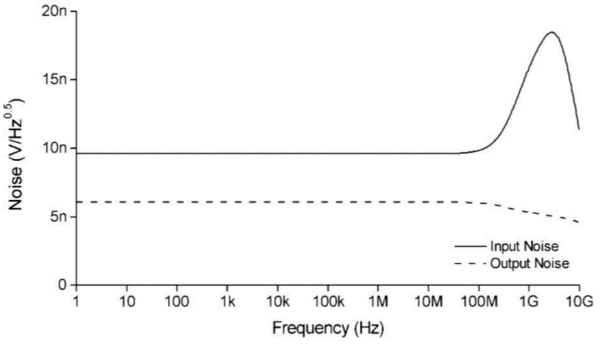

Figure 13. Input and output noise of the first proposed transconductor.

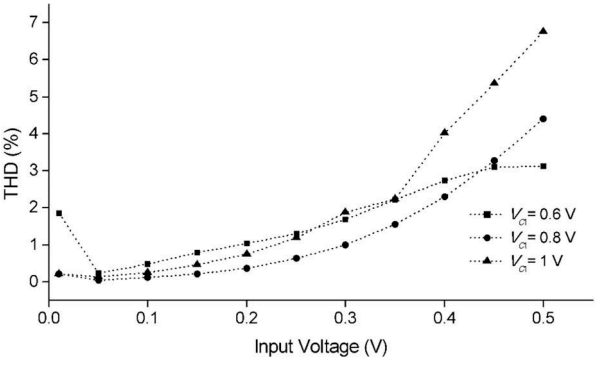

Figure 14. Total harmonic distortion (THD) of the first proposed transconductor.

In order to obtain high input impedance control voltage, M_7 transistor is added to the control voltage terminal of the first proposed transconductor as shown in Figure 15. Aspect ratio of M_7 is selected as $(W/L)_7$ = 15 µm/1 µm. Thus, Figure 16 illustrates the output current of

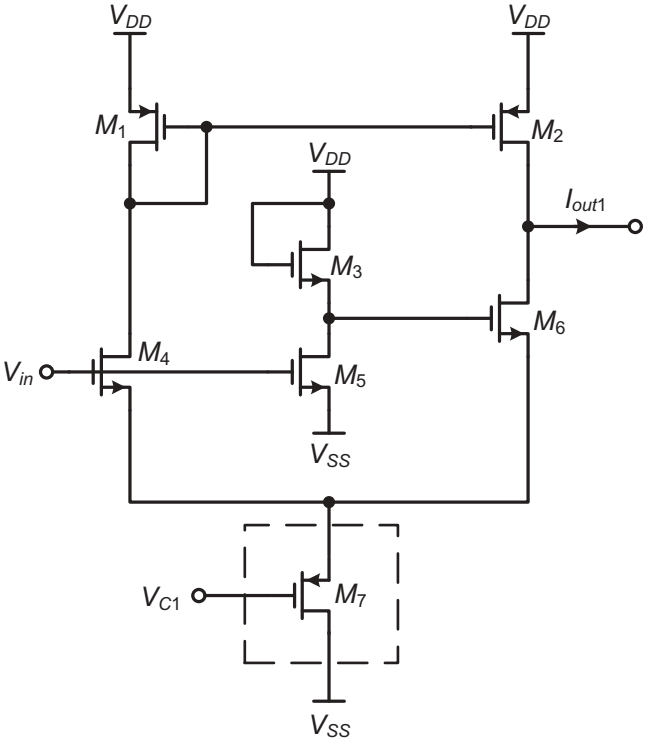

Figure 15. The first proposed transconductor in Figure 3 with high input impedance control voltage terminal.

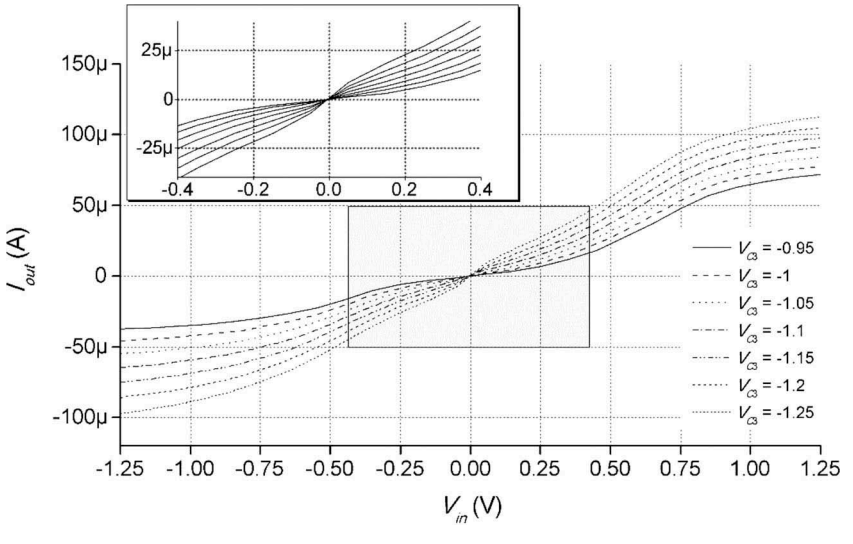

Figure 16. DC transfer characteristics of the first proposed transconductor with high input impedance control voltage terminal in Figure 15.

the first proposed transconductor with high impedance control voltage input in Figure 15 with respect to input voltage where control voltage is changed from −1.25 V to −0.95 V with a step size of 0.05 V.

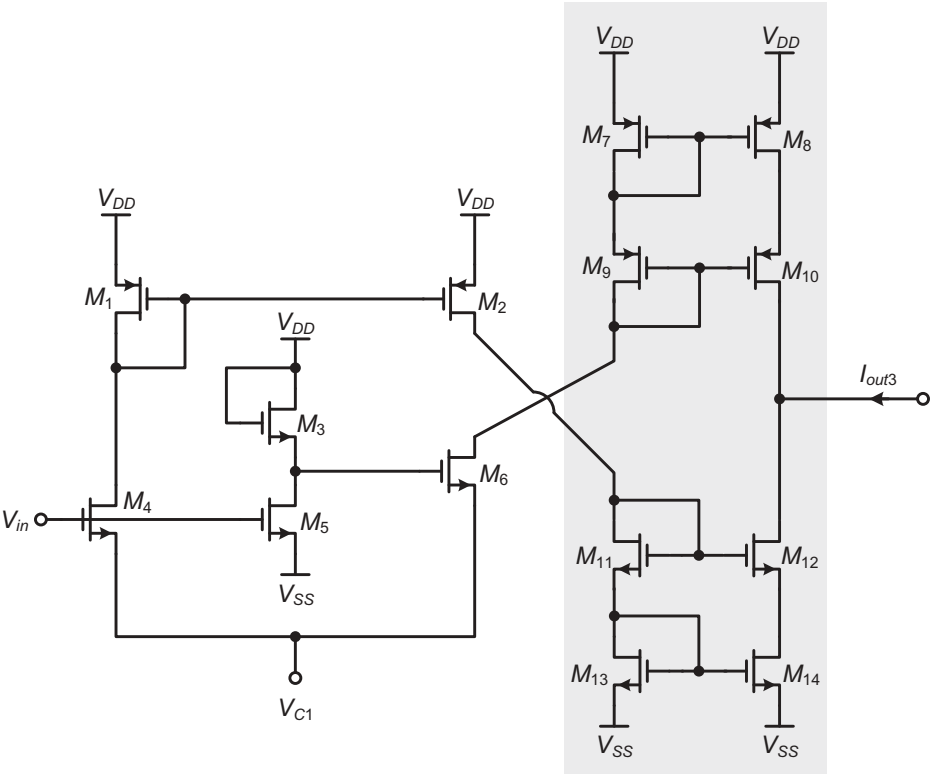

Figure 17. The proposed transconductor with higher output impedance.

The proposed circuit with higher output impedance is given in Figure 17. Aspect ratios of PMOS transistors and NMOS transistors of the proposed transconductor in Figure 17 are selected as $(W/L)_{7-10}$ = 15 µm/1 µm and $(W/L)_{11-14}$ = 5 µm/1 µm, respectively. Figure 18

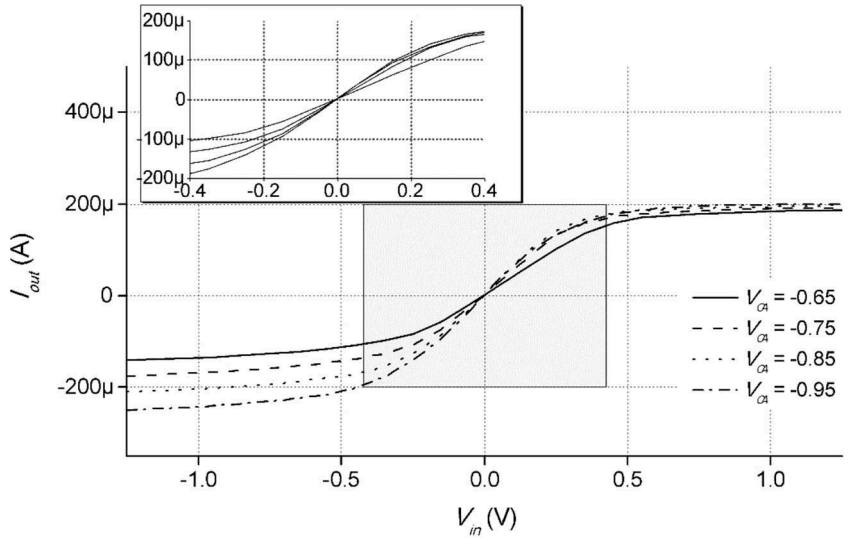

Figure 18. DC transfer characteristics of the first proposed transconductor with higher output impedance in Figure 17.

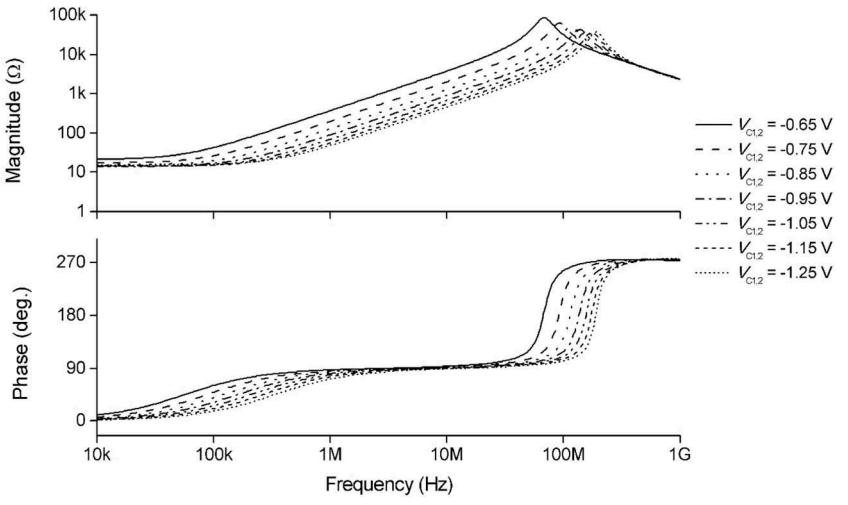

Figure 19. Ideal and simulated magnitudes and phases of the impedance of the positive inductor simulator by changing $V_{C1,2}$.

illustrates the output current of the first proposed transconductor with high output impedance in Figure 17 with respect to input voltage where control voltage (V_{C1}) is changed from −0.95 V to −0.65 V with a step size of 0.1 V. Also, output resistance of the transconductor in Figure 17 is evaluated as

$$R_{out} \cong (g_{m12}r_{o12}r_{o14})//(g_{m10}r_{o8}r_{o10}) \tag{17}$$

Further, magnitudes and phases of the impedances by variation of the control voltages ($V_{C1,2}$) between −1.25 V and −0.65 V for the proposed lossless positive grounded inductor simulator are drawn in Figure 19. Ideal and simulated results are approximately compatible at the frequency range of 500 kHz and 30 MHz.

The robustness of the first proposed circuit is analysed by some simulations. As an example, a complete PVT (process, voltage supply and temperature) analysis is performed to show the performance of the first proposed transconductor in Figure 3. First, varying the width (W) parameter of the NMOS transistors in Figure 3 between 4 µm and 6 µm with a step size of 0.25 µm, the variation of DC transfer characteristics of the first circuit is depicted in Figure 20a. A slight change of V–I characteristic curve slope is obtained in this analysis result. Second, a Monte Carlo analysis is done with 1% Gaussian distribution process variations of threshold voltages all the MOS transistors. This analysis result for DC transfer characteristics of the first proposed transconductor is shown in Figure 20b. The transconductor response is affected by the change of threshold voltages. Third, if symmetrical power supply voltages are varied by 20% between ±1 V and ±1.5 V with a step size of 0.25 V, a considerable change is not seen in DC transfer characteristics of the first proposed transconductor as given in Figure 20c. Finally, a temperature analysis shown in Figure 20d is performed where the temperature is varied between −25°C and 75°C with a step size of 25°C. The DC transfer characteristics variations of the first proposed transconductor are shown in Figure 20d.

The first proposed transconductor in Figure 3 can be realized by six commercially available discreet MOS transistors such as BS250P and 2N7000. BS250P and 2N700 are respectively P-channel and N-channel enhancement type MOS transistors (Vishay Siliconic, 2001; Zetex, 2014). An experimental test is performed applying a sinusoidal input voltage with peak to peak amplitude of 500 mV at 10 kHz. Here, the output current is converted to voltage by a load resistor R_L = 1 kΩ connected to the output terminal of the circuit. The input voltage and

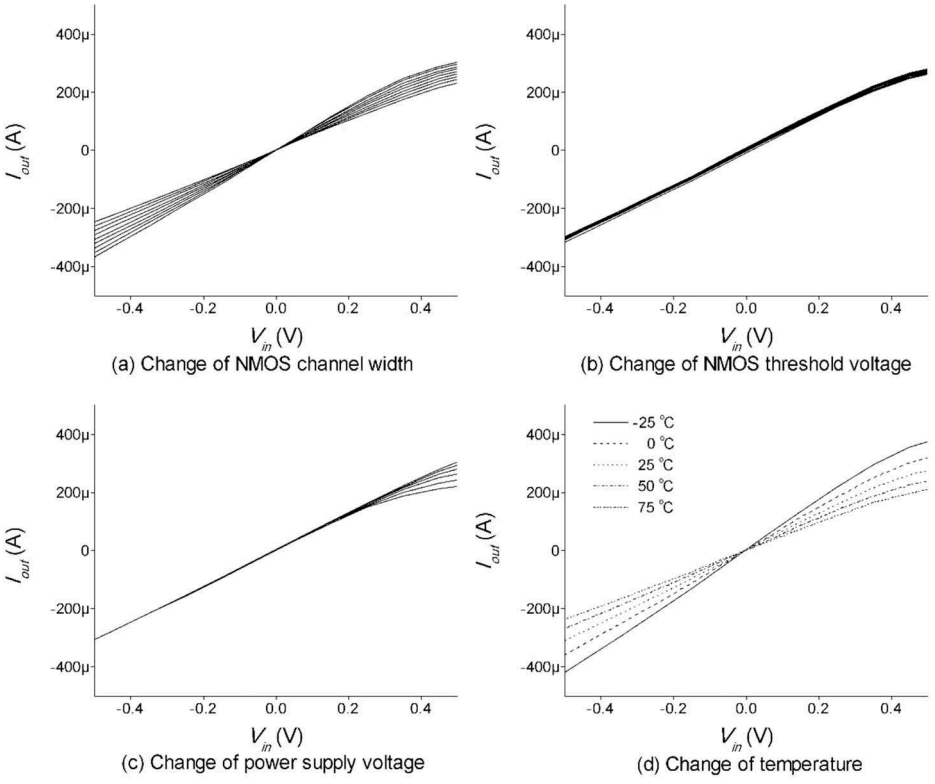

Figure 20. PVT (process, voltage supply and temperature) analysis of the first proposed transconductor. (a) Change of NMOS channel width. (b) Change of NMOS threshold voltage. (c) Change of power supply voltage. (d) Change of temperature.

corresponding output voltage signals are shown in Figure 21. The symmetrical power supply voltages are selected as ±3 V and the control voltage V_{C1} is chosen as 3 V. This work is compared with some open literature transconductor circuits in Table 2.

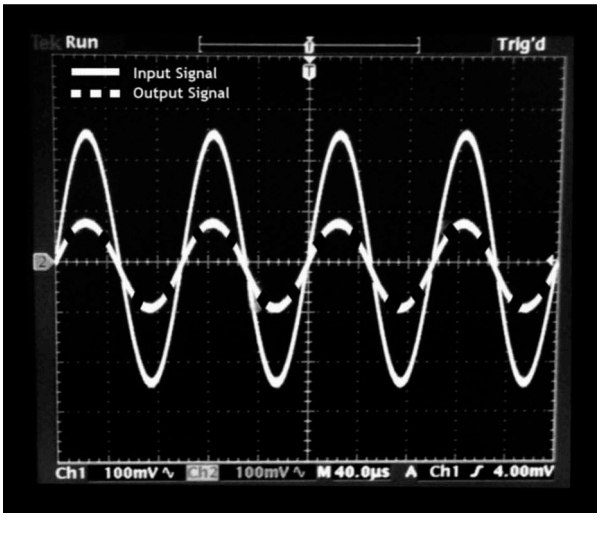

Figure 21. Experimental test result (100 mV/div for both the input and output signals and R_L = 1 kΩ).

Table 2. A comparison of open literature transconductors and this work.

References	Number of transistors	Number of resistors	Number of capacitors	Number of biasing sources	Number of control voltages or currents (typical value)	Unified or specific g_m (S)	Linearity error (%)	Input dynamic range	Tunability range	Technology	Power consumption	Supply voltages
Fayed and Ismail (2005)	12[a]	0	0	0	1 (100 mV–1 V)	≅110 µ (at V_C = 1 V)	2.6% (at V_C = 100 mV)	±900 mV	0 –0.4 V	0.18 µm	418 µW[b]	1.8 V
Gatti et al. (1994)	21	0	2	1	1 (I_1 = 50 µA)	230.7 µ – 242.9 µ	≅4.7%	±1.6 V	I_1 = 10 µA–200 µA	2 µm	12 mW	±5 V
Worapished and Naphaphan (2003)	10	1	0	1	0 (NA)	500 µ (at V_B = 1.35 mA)	NA	±0.4 V	NA	0.35 µm	3.4 mW	2.5 V
Kuo and Leuciuc (2001)	11	0	0	1	1 (NA)	40µ[b]	<1%	±0.5 V	NA	0.35 µm	1 mW	3.3 V
Martinez-Heredia and Torralba (2011)	24	3	2	5	0 (NA)	40 µ	NA	350mV	NA	0.13 µm	126 µW	1.5 V
Mahmoud and Soliman (1999)	30, 20, 12, 20	0	0	1	1 (V_C = 1.4 V, V_C = −0.8 V) or 2 (V_a, V_b)	NA	NA	±1.25 V	NA	2 µm	NA	±2.5 V
Ohbuchi and Matsumoto (2013)	6	0	0	1	1 (I_S = 100 nA)	1.63 µ	1%	0.01 to 0.1 V	<100 nA	0.18 µm	50.8 µW (at G_m (0) = 1.63 µS)	±0.9 V
Tongpoon et al. (2012)	7 or 9	0	0	1	1 (I_o = 10 µA)	60 µA–80 µA or 30 µA–35 µ	<2%	±0.5 V	8 µ–14 µA or7 µA–10 µA	0.18 µm	102.6 µW or 108.3 µW	±0.9 V
Figure 2 in Vlassis and Raikos (2012)	17[a]	0	1	3	1 (I_{T2} = 1µA to 10µA)	16 µ–187 µ (at I_{T2} = 1 µA–10 µA)	3.1%	±0.5 V	1–10 µA	0.18 µm	NA	1.8 V
Torralba et al. (2002)	14	0	0	1	1 (V_C = 1 V)	396 µ–2443 µ (at V_C = 0.8 V–1 V)	NA	±0.6 V	0.8 to 1 V	0.8 µm	4.3 mW	1.5 V
Ismail and Soliman (2000)	23	0	0	2	0 (NA)	NA	NA	±1.5 V	NA	0.5 µm	NA	±1.5 V
Figure 5 in Han (2006)	18	0	0	0	1 (V_C = 1 V)	20 µ ±50% (at V_C = 1 V ± 0.2 V)	NA	±0.3 V	1 V ± 0.2 V	0.18 µm	145 µW	1.8 V
Yamaguchi et al. (2005)	10	0	0	3	1 (V_B = 0.3 V)	10 µS–50 µS (V_B = 0.1 V–0.5 V)	0.5%	±1 V	0.1 to 0.5 V	0.5 µm	NA	NA
Figure 4 in Demosthenous and Panovic (2005)	6	0	0	1	0 (NA)	265.9 µ	1.15%	±300mV	NA	0.8 µm	160 µW	2 V
El-Adawy and Soliman (2000)	22	0	0	0	2 (I_B = 50 µA)	13 µS–90 µS	NA	±1.5 V	20µ to 60µA	1.2 µm	NA	±1.5 V
Nauta (1992)	12	0	1	0	0 (NA)	0.4 mS–1.5 mS[b]	%1	±1 V	NA	3 µm	NA	±2.5 V ±5 V ±10 V
This work	6	0	0	0	1 (V_C = 0.8 V)	343.2 µ–1.08 m	6.85%	±0.5 V	−1.2 to −0.6 V	0.25 µm	1.26 mW	±1.25 V

NA: Non-available.
[a]Used extra output amplifiers.
[b]Calculated for experimental set-up.

5. Conclusion

This article describes two new highly linear tunable transconductor circuits which have voltage input and current output. Both of the proposed transconductors include only six transistors operated in the saturation region. The transconductance of both transconductors can be tuned linearly by a control voltage. Both of the transconductors do not require extra bias currents or voltages. An advantage of all the configurations is their high input and output impedances. As an application of the transconductors, a positive lossless inductor simulator using a grounded capacitor is given. The simulation and experimental test results verify the claimed theory well as expected. However, the difference among ideal, simulation and experimental results can be attributed to non-idealities of the MOS transistors.

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