Indian Journal of Engineering & Materials Sciences
Vol. 21, August 2014, pp. 351-357

A new cascadable CMOS voltage squarer circuit and its application: Four-quadrant analog multiplier

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Received 21 June 2013; accepted 24 June 2014

A new cascadable CMOS based voltage squarer circuit having voltage input/current output and its analog four-quadrant multiplier application are presented. The proposed structure has high input impedance and high output impedance; thus, it can be easily connected to other circuits without requiring any extra buffers. Moreover, its two symmetrical bias voltages have high input impedances; accordingly, bias voltages can be easily connected without requiring additional circuits. Another advantage of the proposed circuit is its low power consumption. It consists of only six MOS transistors. However, it needs several active component matching constraints. Some SPICE simulation and experimental test results are included to confirm the proposed theory.

Keywords: CMOS, Voltage squarer circuit, Four-quadrant analog multiplier

Analog squarer circuits are widely used in some signal processing applications such as image process, modulators, signal generators, frequency dividers and multipliers[1-13]. The squarer circuits are mainly designed by four techniques: voltage input/current output[1-5], current input/current output[7-10], voltage input/voltage output[11-13] and mixed-mode[6].

There are a number of squarer circuits in the related open literature having a large number of components[1,11,12]. A squarer circuit which has voltage input and current output includes an operational amplifier and two nested transistors but transistor imperfections limit the circuit performance[2]. Some circuits require additional components such as adder and subtractor[3]. Several squarer circuits require two symmetrical input sources[4,13]. Additionally, a squarer circuit which has voltage input and current output includes four transistors, however its two symmetrical bias voltages do not have high impedances[5]. Although the configuration in ref.[6] has low total harmonic distortion (THD) variations for applied peak sinusoidal input voltages less than 500 mV, the proposed one has low THD variations for applied peak sinusoidal input voltages less than 1500 mV. Current-mode multiplier applications using squarer circuits are found in refs [9,10,14]. Also, a voltage-mode analog multiplier application has been reported in ref.[15].

In this paper, a new cascadable CMOS voltage squarer circuit which has voltage input/current output and its analog four-quadrant multiplier application are proposed. This circuit has high input impedance and high output impedance; accordingly, it can be easily connected to other circuits without requiring buffers. Also, its two symmetrical bias voltages possess high input impedances; thus, bias voltages can be easily connected without needing extra structures. Another advantage of the proposed circuit is its low power dissipation. The proposed configuration employs only six MOS transistors. Nevertheless, it requires some active component matching conditions. A number of simulation and experimental test results are included to verify the proposed theory.

Proposed CMOS Voltage Squarer

The proposed CMOS voltage squarer circuit is shown in Fig. 1a. It uses only six MOS transistors M_1-M_6, and two bias voltages $\pm V_b$. It is assumed that all the MOS transistors in Fig.1 are worked in saturation region. M_1 and M_2 transistors are used to create a current mirror. The drain currents of the PMOS and NMOS transistors operating in saturation region can be respectively given by the square-law relation as:

$$I_{Dp} = \frac{k_p}{2}\left(V_{SG} - |V_{TP}|\right)^2 \quad \ldots (1a)$$

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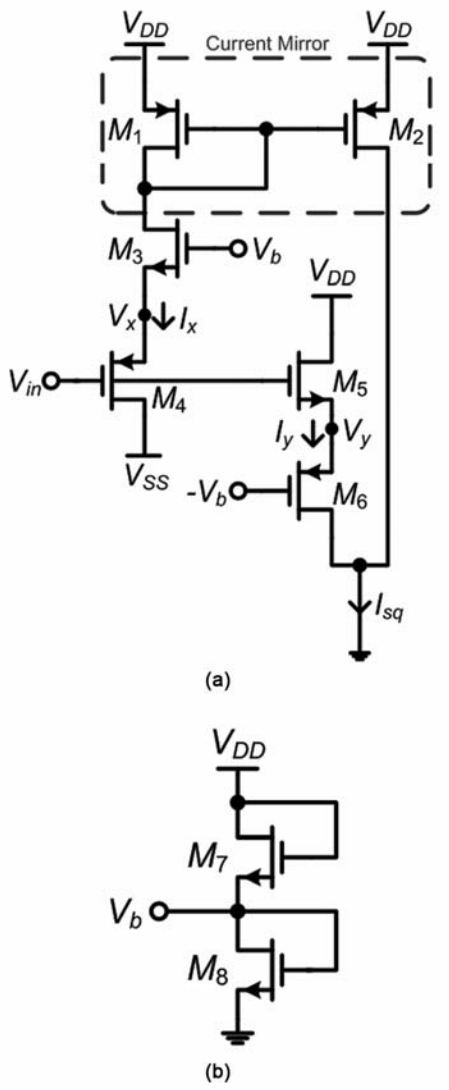

Fig. 1 –Schematic of the (a) proposed squarer circuit and (b) bias voltage generator circuit[16]

$$I_{Dn} = \frac{k_n}{2}\left(V_{GS} - V_{TN}\right)^2 \quad \ldots (1b)$$

where $k_p=\mu_p C_{ox}(W/L)$ and $k_n=\mu_n C_{ox}(W/L)$ are transconductance parameters of the transistors, μ_p and μ_n are respectively mobility of the carrier for PMOS and NMOS transistors, C_{ox} is the gate oxide capacitance per unit area, W is the channel width, L is the channel length. Also, V_{GS} is the gate-to-source voltage, V_{SG} is the source-to-gate voltage, V_{TP} and V_{TN} are respectively threshold voltages of the PMOS and NMOS transistors. The drain currents of the transistors M_3-M_6 in can be respectively expressed as:

$$I_{D3} = \frac{k_n}{2}\left(V_b - V_x - V_{TN}\right)^2 \quad \ldots (2a)$$

$$I_{D4} = \frac{k_p}{2}\left(V_x - V_{in} - \left|V_{TP}\right|\right)^2 \quad \ldots (2b)$$

$$I_{D5} = \frac{k_n}{2}\left(V_{in} - V_y - V_{TN}\right)^2 \quad \ldots (2c)$$

$$I_{D6} = \frac{k_p}{2}\left(V_y + V_b - \left|V_{TP}\right|\right)^2 \quad \ldots (2d)$$

Transconductance parameters of the transistors M_1 through M_6 are assumed to be equal to K, the current I_x flowing downward through M_3 and M_4, and the current I_y flowing downward through M_5 and M_6 can be written as:

$$I_x = \frac{K}{2}\left(V_b - V_x - V_{TN}\right)^2 = \frac{K}{2}\left(V_x - V_{in} - \left|V_{TP}\right|\right)^2 \quad \ldots (3a)$$

$$I_y = \frac{K}{2}\left(V_{in} - V_y - V_{TN}\right)^2 = \frac{K}{2}\left(V_y + V_b - \left|V_{TP}\right|\right)^2 \quad \ldots (3b)$$

A bias voltage generator circuit in Fig. 1b[16] can be used to provide the bias voltage for the proposed circuit. The biasing voltage V_b satisfies the following equation:

$$V_b = \left|V_{TP}\right| + V_{TN} \quad \ldots (4)$$

V_b can be generated by selecting $k_{n8} << k_{n7}$. In order to obtain $-V_b$, two PMOS transistors and V_{SS} can be used. Eliminating $K/2$ and square-rooting both sides of Eqs (3a) and (3b), the followings are respectively obtained:

$$V_b - V_x - V_{TN} = V_x - V_{in} - \left|V_{TP}\right| \quad \ldots (5a)$$

$$V_{in} - V_y - V_{TN} = V_y + V_b - \left|V_{TP}\right| \quad \ldots (5b)$$

Substituting Eq. (4) into Eqs (5a) and (5b), the followings are obtained:

$$\left|V_{TP}\right| + V_{TN} - V_x - V_{TN} = V_x - V_{in} - \left|V_{TP}\right| \quad \ldots (6a)$$

$$V_{in} - V_y - V_{TN} = V_y + \left|V_{TP}\right| + V_{TN} - \left|V_{TP}\right| \quad \ldots (6b)$$

Eliminating V_{TN} and $|V_{TP}|$, the voltages V_x and V_y are evaluated as:

$$V_x = \frac{V_{in}}{2} + \left|V_{TP}\right| \quad \ldots (7a)$$

$$V_y = \frac{V_{in}}{2} - V_{TN} \quad \ldots (7b)$$

The output current I_{sq} of proposed squarer circuit in can be expressed as:

$$I_{sq} = I_x + I_y \quad \ldots (8)$$

or

$$I_{sq} = \frac{K}{2}\left(V_x - V_{in} - |V_{TP}|\right)^2 + \frac{K}{2}\left(V_{in} - V_y - V_{TN}\right)^2 \quad \ldots (9)$$

Substituting Eqs (7a) and (7b) into Eq. (9), I_{sq} can be obtained as:

$$I_{sq} = \frac{K}{4}V_{in}^2 \quad \ldots (10)$$

Thus, the output current is related to V_{in}^2 by a factor of $K/4$.

Application of Analog Four-Quadrant Multiplier

The operation principle of the developed multiplier is based on the square-difference identity given as follows:

$$(x+y)^2 - (x-y)^2 = 4xy \quad \ldots (11)$$

The developed analog multiplier block diagram is shown in Fig. 2. It is implemented by using two squarer circuits in Fig. 1a. Input signals of the squarer circuits are respectively V_1+V_2 and V_1-V_2. Here, V_1 and V_2 refer to input voltage signals to be multiplied by each other. In order to achieve multiplication, one adder and one subtractor circuits are required[17]. Output current of the developed multiplier is calculated as follows:

$$I_{out} = \frac{K}{4}\left(V_1 + V_2\right)^2 - \frac{K}{4}\left(V_1 - V_2\right)^2 = KV_1V_2 \quad \ldots (12)$$

Simulation Results

Simulations are performed by using level 7 0.25-µm Taiwan Semiconductor Manufacturing Company, Ltd. (TSMC) CMOS technology parameters given in ref.[18] where output of the squarer is connected to ground in SPICE simulations. Also, the aspect ratios of the MOS transistors are given in Table 1. Some technology parameters are given as: V_{TN0} = 0.38 V, V_{TP0} = –0.57 V, μ_{0N} = 294.41 cm^2/V.s, μ_{0P} = 104.40 cm^2/V.s and T_{OX} = 5.7 nm.

The symmetrical DC power supply voltages of the circuit in Fig. 1a are chosen as ±1.25 V. Besides, bias voltage V_b is approximately 0.9 V. A sinusoidal voltage signal with 125 mV peak value at 1 MHz is applied to the input of the proposed squarer circuit in Fig. 1. The output characteristics of the squarer circuit are shown in Fig. 3. It

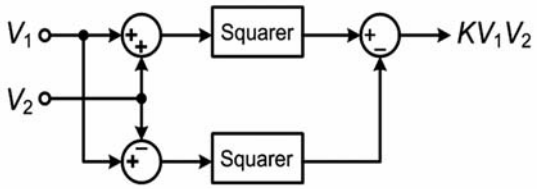

Fig. 2 – Developed multiplier block diagram

Table 1 – Dimensions of the MOS transistors

Type	W (µm)/L (µm)
PMOS transistors M_1, M_2, M_4, M_6	21/0.5
NMOS transistors M_3, M_5	7/0.5

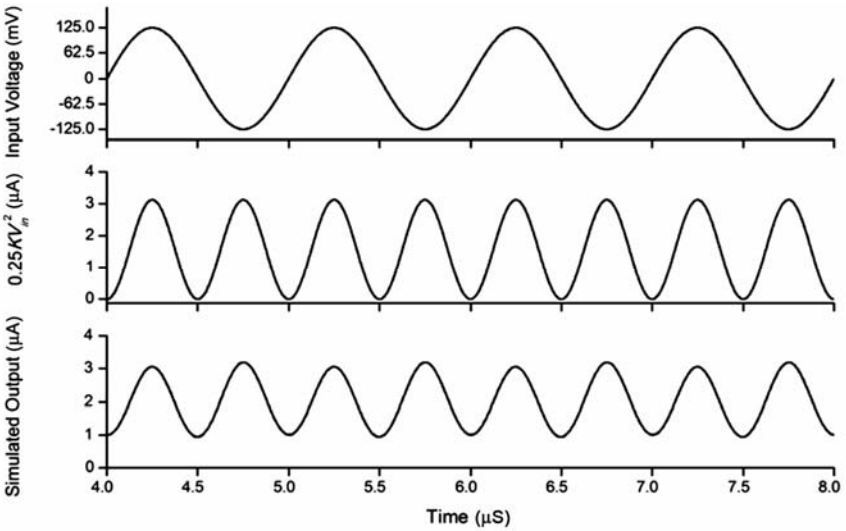

Fig. 3 – The input and corresponding output characteristics of the squarer circuit

is observed from Fig. 3 that the simulated output current of the squarer circuit has a very small DC offset current about 1 µA due to non-idealities of MOS transistors.

After fifty runs, a Monte Carlo simulation by changing 1% Gaussian variation of V_{TP} and V_{TN} parameters of all the MOS transistors is achieved. Also, the result is shown in Fig. 4 where the circuit is sensitive to variation of threshold voltages. If input voltage is high enough, the threshold voltage variations can be ignored. Only the widths of M_3 and M_5 transistors in Fig. 1a are varied between 5 µm and 8 µm by a step size of 0.25 µm. The ideal and simulated outputs are drawn in Fig. 5 Here, the proposed squarer circuit is much less affected from the variations of MOS transistors dimensions. Applying a sinusoidal signal with 125 mV peak value at 1 MHz, the bias voltages (V_b and $-V_b$) are varied between 0.87 V to 0.93 V. The ideal and simulated output responses are drawn in Fig. 6. As shown in Fig. 6, a DC offset voltage occurs at the output signal by varying V_b and $-V_b$.

The total power dissipation of the circuit is found as approximately 4.02 µW, which is obtained from SPICE simulations. Varying the amplitude peak value of the input sinusoidal signal at 1 MHz, THD values calculated by SPICE are depicted in Fig. 7. In this simulation, the bias voltages are taken as ±0.9 V. Minimum THD value is found as 1.62% at 125 mV. The fast Fourier transform (FFT) graph of the proposed circuit at frequency of 2 MHz is given in Fig. 8. Fig. 9 shows the results of transient analysis of the analog four-quadrant multiplier circuit. In this simulation, $V_1(t) = 250\times10^{-3}\sin(2\pi\times5\times10^6)$, $V_2(t) = 50\times10^{-3}\sin(2\pi\times30\times10^6)$ and K = 363.48 µA/V^2 are selected. A load resistor, R = 1 kΩ is connected to the output terminal of multiplier circuit to obtain the multiplier output voltage signal, therefore output voltage can be written as $V_{out} = KV_1(t)V_2(t)R$.

It is observed from simulation results in Figs 3-9 that the ideal and simulated responses are close to

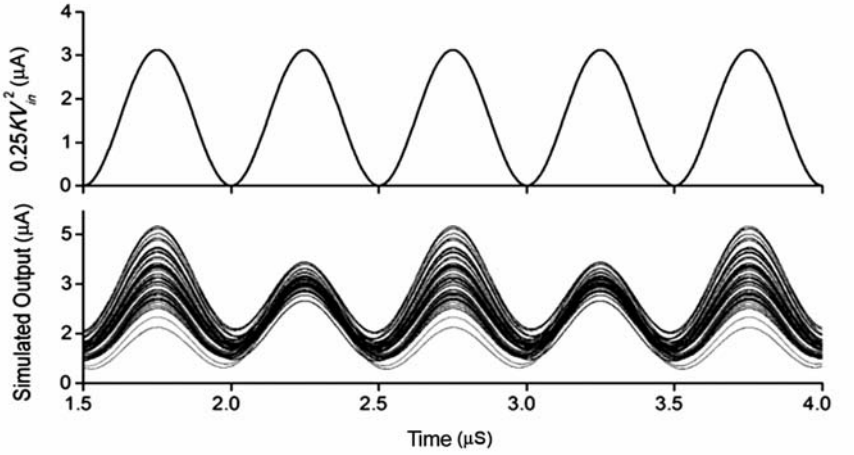

Fig. 4 – A Monte Carlo analysis with variation of threshold voltages

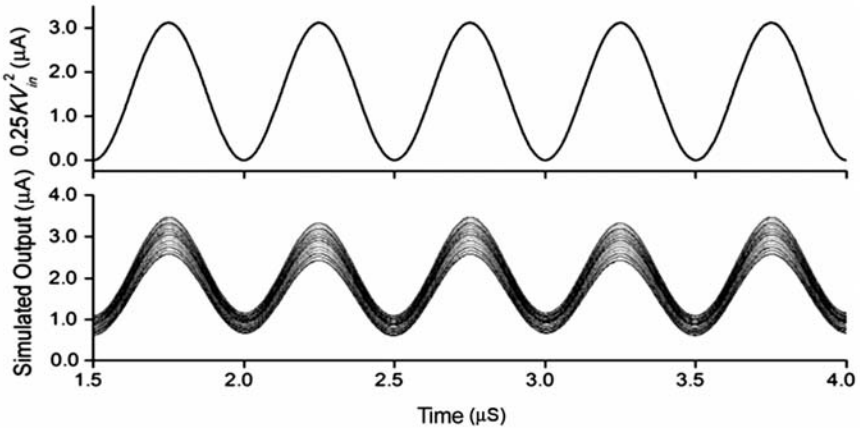

Fig. 5 – Time domain responses for variation of width parameters of M_3 and M_5 transistors

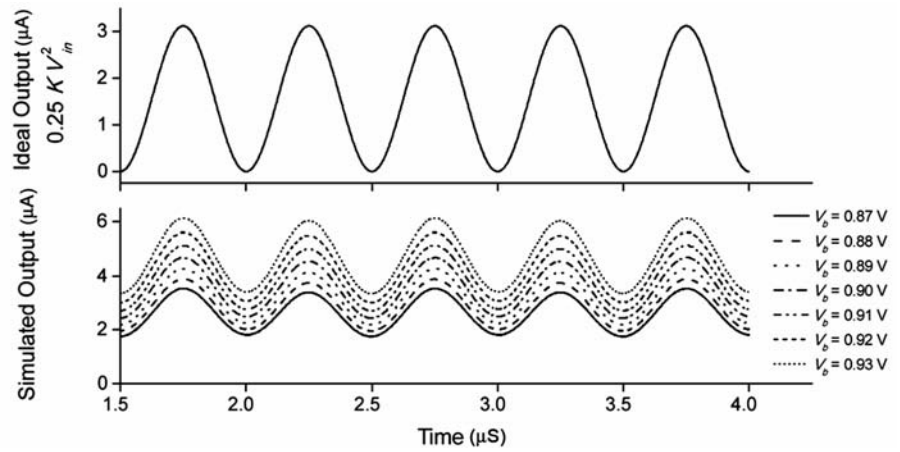

Fig. 6 – Time domain squarer ideal and simulated response for the variation of bias voltages, $\pm V_b$

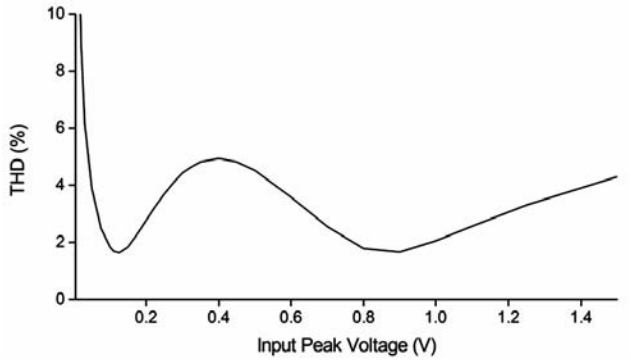

Fig. 7 – THD versus peak value of the applied sinusoidal signal

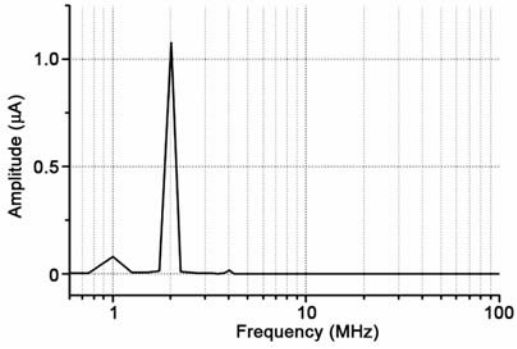

Fig. 8 – FFT graph of the proposed circuit at 2 MHz

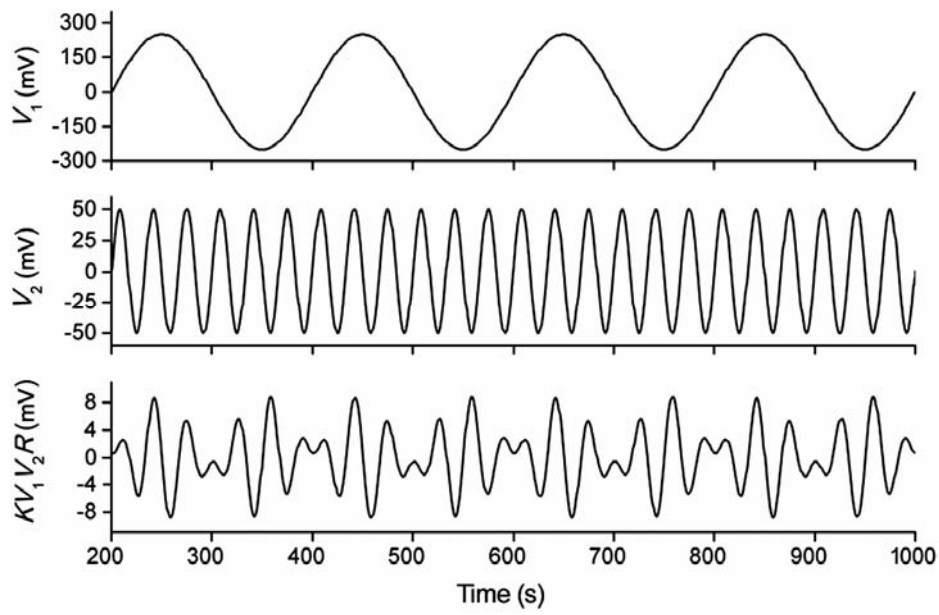

Fig. 9 – Inputs and corresponding output voltage of the multiplier circuit

Table 2 — Comparison of the proposed and previously published squarer circuits

References	# of MOSFET	High input/ output impedances	# of bias voltage(s) and current(s)	High input impedance bias voltage(s)	Supply voltages	Power consumption	Technology
[1]	20	Yes/ Yes	3	Yes	±5 V	NA	3.5 µm
[2]	4 MOS + 1 OA	Yes/ Yes	0	-	+5 V	NA	MO414, MO421
[3]	10	Yes/ Yes	1	Yes	±3 V	NA	1.2 µm
[4]*	6	Yes/ No	5	Yes	±1.5 V	1.28 mW	0.35 µm
[5]	4	Yes/ Yes	2	No	V_{TN}, V_{TP}	0.08 µW	0.18 µm
[6]	4	Yes/ No	0	-	±2 V	NA	0.5 µm
This work	6	Yes/ Yes	2	Yes	±1.25 V	4.02 µW	0.25 µm

* Requires symmetrical inputs, OA: Operational Amplifier, NA: not available

each other whereas the slight discrepancy between them can be attributed to non-idealities of the MOS transistors such as internal parasitic capacitors. Therefore, the output distortion rises as the frequency increases.

THD variations for applied peak input voltage between 25 mV–225 mV and 650 mV–1.25 V as seen in Fig. 7 are less than 3% which can be acceptable. Also, by adding a current mirror with two NMOS transistors to the output, the output impedance of the squarer can be performed higher whereas THD a bit increases. In Fig. 8, the applied input voltage to the proposed squarer is 125 mV peak sinusoidal signal at 1 MHz frequency value, fundamental frequency of the output current is at 2 MHz as expected. Also, in Fig. 9, simulated output current is obtained as multiplication of V_1 and V_2 input voltage signals with coefficient K. On the other hand, a comparison table for voltage input/current output squarer circuits is given in Table 2.

Experimental Results

In order to achieve an experimental test, the proposed squarer in Fig. 1a is employed by commercially available MOS transistors such as CD4007s. A load resistor of 750 kΩ is connected to the output terminal to obtain output voltage signal. Bias voltage sources ($\pm V_b$) are chosen as ±5 V. Also, symmetrical power supply voltages are selected as ±6 V. Applying a sinusoidal input signal with 5 V peak value at 750 kHz to the proposed squarer circuit, the time domain sinusoidal input and corresponding output voltage signals are demonstrated in Fig. 10.

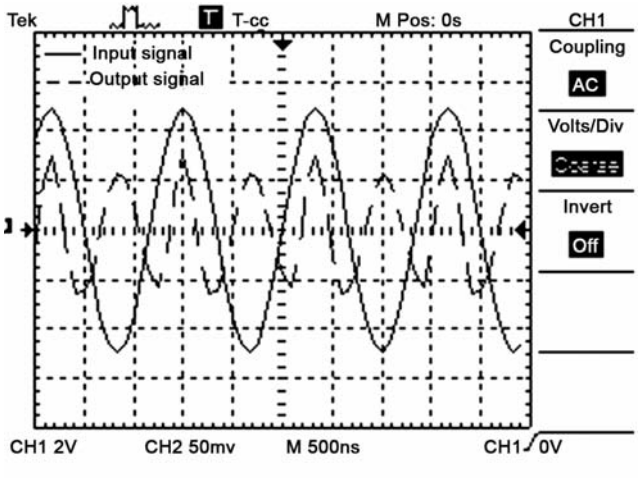

Fig. 10 – Time domain input and output responses of the proposed squarer

It is observed from simulation and experimental test results that the ideal, simulation and experimental test results are close to themselves whereas the slight discrepancy among them can be attributed to non-idealities of the MOS transistors. Also, parasitic capacitors and resistors of the board where experimental test is performed affect the performance of the proposed squarer circuit.

Conclusions

A new CMOS based voltage squarer circuit having voltage input/current output and its analog four-quadrant multiplier application are proposed in this paper. The proposed circuit has high input impedance and high output impedance resulting in easy cascadability with other circuits. Furthermore, its two symmetrical bias voltages have high input impedances; accordingly, bias voltages can be easily connected without requiring additional topologies. Another advantage of the proposed voltage squarer is its low power dissipation. It is composed of only six CMOS transistors yielding no large silicon area in integrated circuit technology. Nonetheless, it requires some active component matching conditions. A number of included SPICE simulation and experimental test results confirm the proposed theory well.

Acknowledgements

This work is partly funded by Pamukkale University Scientific Research Project (BAP) Management Office by grant number of 2012FBE033.

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