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A new wideband electronically tunable grounded resistor employing only three MOS transistors

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Abstract: In this paper, a new wideband electronically tunable grounded resistor, namely a grounded voltage controlled resistor (GVCR) including only three MOS transistors, is suggested. The proposed GVCR, without requiring any additional bias currents and voltages, has only one control voltage. Linearity analysis for the proposed GVCR is given. A new second-order multifunctional filter using two differential voltage current conveyors is also included as an application example. Some postlayout simulation results with SPICE are included to show the performance, workability, and effectiveness.

Key words: Tunable resistor, MOS transistor, body effect, channel length modulation, differential voltage current conveyor, multifunctional filter

1. Introduction

Grounded voltage controlled resistors (GVCRs), namely electronically tunable grounded resistors, reported in the related literature can be adjusted via control voltage(s) in CMOS technology [1–6]. The complete circuit of the GVCR in [1] uses five MOS transistors, whereas the proposed one in this study employs only three MOS transistors. The GVCR of [2] consists of nine MOS transistors. Furthermore, it needs a bias voltage that is implemented with additional elements [7]. The GVCR of [3] uses two MOS transistors, both of which operate in the saturation region. Nevertheless, the circuits of [3–5] have two symmetrical control voltages in opposite signs, which are constructed by extra components. A grounded current-controlled resistor was designed in [6] with three MOS transistors that needs at least one extra MOS transistor to be tuned by a control voltage. The circuits of [8] and [9] use BJTs, which are temperature-dependent. The grounded resistor circuit in [10] consists of a single JFET and a current feedback operational amplifier (CFOA). The grounded tunable resistor given in [11] uses floating-gate MOS transistors. As stated in [12], some voltage-controlled resistor circuits are given in [13–20]. These configurations were employed for the nonlinearity cancellation by the same principle where the same active devices (CFOAs) were used. The floating resistor circuits of [21–25] also include a number of MOS transistors. Apart from this, some tunable circuits that employ active building blocks are given in the literature [26].

In this paper, a new wideband linear GVCR containing only three MOS transistors, one NMOS transistor in the linear region and two MOS transistors in the saturation region, is proposed. It has a single control voltage

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for electronically tuning its linear resistive values. It does not require any bias currents and voltages, whereas it requires a single matching condition. A tunable second-order multifunctional filter using two differential voltage current conveyors (DVCCs) and only grounded passive elements is given as an application example. Some postlayout simulation results with SPICE are included to confirm the theory.

2. Grounded voltage controlled resistor

The input-output relationship of an active device can be expressed as

$$I_{in} = f(V_{in}) = \sum_{j=0}^{\infty} \left(a_j V_{in}^j \right), \tag{1}$$

where I_{in} is input current and V_{in} is corresponding input (output) voltage of the active device. Ideally, a GVCR electronically tuned via control voltage(s) is defined by $I_{in} = a_1 V_{in}$, where a_1 is a function of control voltage(s).

The electrical symbol of the GVCR with one control voltage and its equivalent circuit [27] are respectively given in Figures 1 and 2. In Figure 2, R_{eq} is an equivalent resistor and C_p is a parasitic capacitor. The impedance in Figure 2 is evaluated as follows.

$$\begin{aligned} Z_{in}(\omega) &= \tfrac{V_{in}}{I_{in}} = \tfrac{R_{eq}}{1+j\omega R_{eq} C_p} \\ &= \tfrac{R_{eq}}{1+\frac{j\omega}{\omega_C}} \end{aligned} \tag{2}$$

Here, $\omega_C = 1 \,/\, (R_{eq} C_p)$ is a pole frequency. For proper operation of the GVCR, $f << \omega_C \,/\, (2\ \pi)$ should be chosen. Moreover, R_{eq} is controlled through V_C.

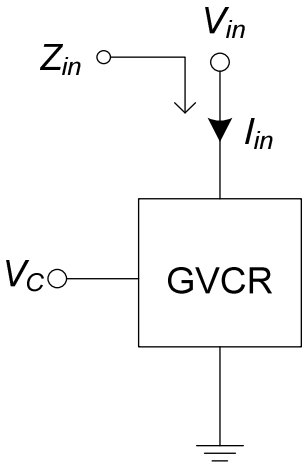

Figure 1. Electrical symbol of a GVCR with one control voltage, V_C.

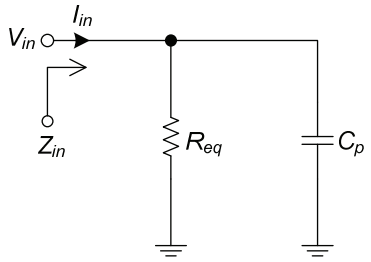

Figure 2. Equivalent circuit of the GVCR in Figure 1 [27].

3. Proposed tunable resistor

The proposed MOS transistor-based wideband linear GVCR circuit is shown in Figure 3. It includes three MOS transistors: PMOS transistor M_1 provides only DC current. NMOS transistors M_2 and M_3 operate in the linear and saturation regions, respectively.

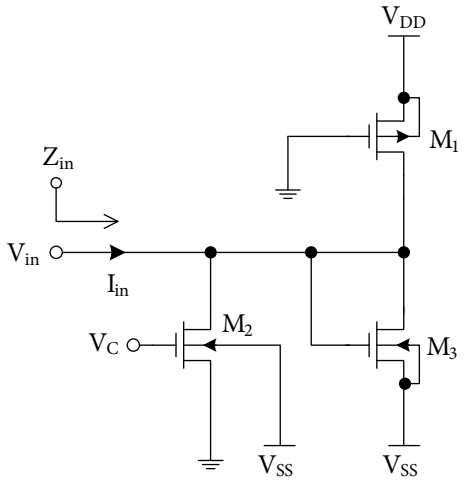

Figure 3. Proposed GVCR composed of only three MOS transistors.

The drain currents I_1, I_2, and I_3 in Figure 3 can be respectively found as

$$I_1 = \frac{k_{p1}}{2}\left(V_{DD} - |V_{TP}|\right)^2, \tag{3a}$$

$$I_2 = k_{n2}\left(\left(V_C - V_{TN}\right)V_{in} - \frac{V_{in}^2}{2}\right), \tag{3b}$$

$$I_3 = \frac{k_{n3}}{2}\left(V_{in} - V_{TN} - V_{SS}\right)^2, \tag{3c}$$

where k_{p1} and k_{ni} $(i = 2, 3)$ are transconductance parameters of the PMOS and NMOS transistors, respectively. V_{DD} and V_{SS} are the positive and negative power supply voltages, respectively. For proper operation of the proposed GVCR, one must choose $k_{n2} = k_{n3} = k_n$. Large signal analysis is performed in this paper. Finally, I_{in} is obtained as follows.

$$\begin{aligned} I_{in} &= -I_1 + I_2 + I_3 \\ &= -\tfrac{k_{p1}}{2}\left(V_{DD} - |V_{TP}|\right)^2 + k_n\left(\left(V_C - V_{TN}\right)V_{in} - \tfrac{V_{in}^2}{2}\right) + \tfrac{k_n}{2}\left(V_{in} - V_{TN} - V_{SS}\right)^2 \\ &= -\tfrac{k_{p1}}{2}\left(V_{DD} - |V_{TP}|\right)^2 + \tfrac{k_n}{2}\left(-V_{TN} - V_{SS}\right)^2 + k_n\left(V_C - 2V_{TN} - V_{SS}\right)V_{in} \end{aligned} \tag{4}$$

If one chooses,

$$\frac{k_{p1}}{2}\left(V_{DD} - |V_{TP}|\right)^2 = \frac{k_n}{2}\left(-V_{TN} - V_{SS}\right)^2, \tag{5}$$

and then Eq. (4) simplifies to

$$I_{in} = k_n\left(V_C - 2V_{TN} - V_{SS}\right)V_{in}. \tag{6}$$

From Eq. (6), the equivalent positive resistance is evaluated as in the following:

$$R_{eq} = \frac{V_{in}}{I_{in}} = \frac{1}{k_n(V_C - V_{SS} - 2V_{TN})}, \tag{7}$$

where V_C is control voltage. The following constraints must be satisfied for proper operation of the proposed GVCR.

$$\begin{cases} V_{in} - V_{TN} - V_{SS} \geq 0 \\ V_{in} \leq |V_{TP}| \qquad\qquad \forall V_{in} \\ V_C - V_{TN} \geq V_{in} \end{cases} \tag{8}$$

It is seen from Eq. (8) that V_C must be chosen as positive. Note that due to the body effects of the second MOS transistor, nonlinearity may occur, which can be considerably reduced by connecting the body to V_{SS}. The M_1 and M_3 transistors also suffer from early voltage effects yielding nonlinearity, which is discussed in the next section.

4. Linearity analysis

Transistors and other semiconductor devices are nonlinear, while resistors and capacitors are linear devices. However, the devices with nonlinear elements can operate linearly if the signal is limited to a low level. Therefore, in Eq. (1), if $I_{in} = a_1 V_{in}$, the device is linear, or if

$$|a_1 V_{in}| >> \left| a_j V_{in}^j \right| \; j = 0 \text{ and } j = 2, 3, 4..., \tag{9}$$

the device can be considered as linear. If second-order effects (body and channel length modulation ones) are ignored, the proposed GVCR is also linear like previously published ones [1–6]. On the other hand, considering the body effect, the threshold voltages of NMOS and PMOS transistors are respectively expressed as

$$V_{TN} = V_{TN0} + \gamma_n \left(\sqrt{|2\varphi_{Fn}| + V_{SBn}} - \sqrt{|2\varphi_{Fn}|} \right), \tag{10a}$$

$$V_{TP} = V_{TP0} - \gamma_p \left(\sqrt{|2\varphi_{Fp}| + V_{BSp}} - \sqrt{|2\varphi_{Fp}|} \right), \tag{10b}$$

where φ_{Fn} and φ_{Fp} are Fermi voltages for NMOS and PMOS transistors, respectively. V_{SBn} and V_{BSp} are source to bulk and bulk to source voltages for NMOS and PMOS transistors, respectively. The threshold voltages of M_1 and M_3 of the realized GVCR in Figure 3 (all the bulks are connected to relevant power supply voltages) are

$$V_{TP1} = V_{TP0}, \tag{11a}$$

$$V_{TN3} = V_{TN0}. \tag{11b}$$

However, if $V_{in} > 0$, from Figure 3, V_{TN2} can be evaluated as

$$V_{TN2} = V_{TN0} + \gamma_n \left(\sqrt{|2\varphi_{Fn}| - V_{SS}} - \sqrt{|2\varphi_{Fn}|} \right). \tag{12}$$

Similarly, if $V_{in} < 0$, V_{TN2} can be computed as

$$V_{TN2} = V_{TN0} + \gamma_n \left(\sqrt{|2\varphi_{Fn}| + V_{in} - V_{SS}} - \sqrt{|2\varphi_{Fn}|} \right). \tag{13}$$

It is seen from Eq. (13) that V_{in} must be chosen sufficiently small for linearity. In other words,

$$|V_{in}| << |2\varphi_{Fn}| - V_{SS}. \tag{14}$$

Considering channel length modulation, $I_1 - I_3$ can be obtained as

$$I_1 = \frac{k_{p1}}{2}\left(V_{DD} - |V_{TP}|\right)^2\left(1 + \lambda_p(V_{DD} - V_{in})\right), \tag{15a}$$

$$I_2 = k_{n2}\left(\left(V_C - V_{TN}\right)V_{in} - \frac{V_{in}^2}{2}\right), \tag{15b}$$

$$I_3 = \frac{k_{n3}}{2}\left(V_{in} - V_{TN} - V_{SS}\right)^2\left(1 + \lambda_n(V_{in} - V_{SS})\right). \tag{15c}$$

Finally, $I_{in} = -I_1 + I_2 + I_3$ is obtained as

$$I_{in} = a_0 + a_1 V_{in} + a_2 V_{in}^2 + a_3 V_{in}^3, \tag{16}$$

where

$$\begin{aligned}
a_0 &= \tfrac{k_{n3}}{2}\left(-V_{TN} - V_{SS}\right)^2\left(1 - \lambda_n V_{SS}\right) - \tfrac{k_{p1}}{2}\left(V_{DD} - |V_{TP}|\right)^2\left(1 + \lambda_p V_{DD}\right)\\
a_1 &= -\tfrac{k_{p1}}{2}\left(V_{DD} - |V_{TP}|\right)^2\lambda_p + k_{n2}\left(V_C - V_{TN}\right) + \tfrac{k_{n3}}{2}\left(-V_{TN} - V_{SS}\right)^2\lambda_n + k_{n3}\left(-V_{TN} - V_{SS}\right)\left(1 - \lambda_n V_{SS}\right)\\
a_2 &= -\tfrac{k_{n2}}{2} + \tfrac{k_{n3}}{2}\left(1 - \lambda_n V_{SS}\right) + k_{n3}\left(-V_{TN} - V_{SS}\right)\lambda_n\\
a_3 &= \tfrac{k_{n3}}{2}\lambda_n
\end{aligned} \tag{17}$$

are obtained. It is desired that a_0, a_2, and a_3 be small enough. Therefore, λ_n and λ_p in Eq. (17) can be made as small as possible by choosing channel length of the MOS transistors in Figure 3 as large as possible [28]. Furthermore, a_0 can be approximately set to zero by adjusting the aspect ratio of M_1.

5. Simulation results

Postlayout simulations of the proposed GVCR based on level 7, 0.25 μ m TSMC CMOS technology parameters with $\pm$ 1.25 V symmetrical DC power supply voltages are accomplished by using the SPICE program. As a result, the aspect ratios of the MOS transistors used in the realization of the proposed GVCR in Figure 3 are selected in all the simulations as follows: $(W\ /\ L)_1 = 37.5\ \mu$ m / 2.5 μ m and $(W\ /\ L)_2 = (W\ /\ L)_3 = 6.5\ \mu$ m / 2.5 μ m, where all the bulks of the MOS transistors are connected to relevant power supply voltages, both bulks of the NMOS transistors are connected to V_{SS}, and the bulk of the PMOS transistor is connected to V_{DD}. In simulations, postlayout PMOS transistor geometry parameters are AD = 8.4375 $\times$ 10^{-11}, AS = 8.4375 $\times$ 10^{-11}, PD = 7.95 $\times$ 10^{-5}, and PS = 7.95 $\times$ 10^{-5}. Postlayout NMOS transistor geometry parameters are AD = 1.3 $\times$ 10^{-11}, AS = 1.3 $\times$ 10^{-11}, PD = 1.7 $\times$ 10^{-5}, and PS = 1.7 $\times$ 10^{-5}. The control voltage, V_C, is chosen as 1.25 V, resulting in $R_{eq} \cong 1.33$ k Ω and a pole of $f_C \cong 443$ MHz. Thus, the proposed GVCR can be operated properly up to a frequency of 44.3 MHz [29].

The total power dissipation for $V_C = 1.25$ V is found as 0.44 mW. Note that power dissipation reduces considerably with lowered power supply voltages but dynamic range is also reduced. Output voltages versus input currents are given in Figure 4, where V_C is selected as 1.25 V ($R_{eq} \cong 1.33$ k Ω), 1.1 V ($R_{eq} \cong 1.5$ k Ω), 0.95 V ($R_{eq} \cong 1.72$ k Ω), 0.8 V ($R_{eq} \cong 2.03$ k Ω), and 0.65 V ($R_{eq} \cong 2.39$ k Ω), separately. The proposed GVCR can be operated properly for $V_C \geq 0.65$ V. Input voltages versus input currents regarding the

Shichman–Hodges [30] model are depicted in Figure 5. Here, V_C is selected as 2.5 V ($R_{eq} \cong 675.5\ \Omega$), 2.2 V ($R_{eq} \cong 730.8\ \Omega$), 1.9 V ($R_{eq} \cong 796\ \Omega$), 1.6 V ($R_{eq} \cong 874\ \Omega$), and 1.3 V ($R_{eq} \cong 969\ \Omega$), separately. Level 1 MOS transistor parameters with $\pm$ 2.5 V symmetrical power supply voltages are specially used only for this simulation [31]. Additionally, $(W\ /\ L)_1 = 25\ \mu$ m / 2.5 μ m and $(W\ /\ L)_2 = (W\ /\ L)_3 = 6.5\ \mu$ m / 2.5 μ m are selected. Input voltages versus input currents as given in Eq. (16) by changing only λ ($\lambda_n = \lambda_p$ is chosen for simplicity) of the MOS transistors are shown in Figure 6. In this simulation, $V_C = 1.25$ V, $k_n = 1$ mA/V^2, $V_{DD} = -V_{SS} = 1.25$ V, $V_{TN} = 0.37$ V, and $V_{TP} = -0.49$ V are selected as an example.

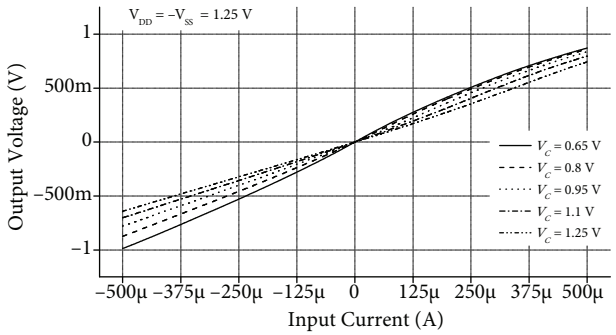

Figure 4. Output voltages against input currents.

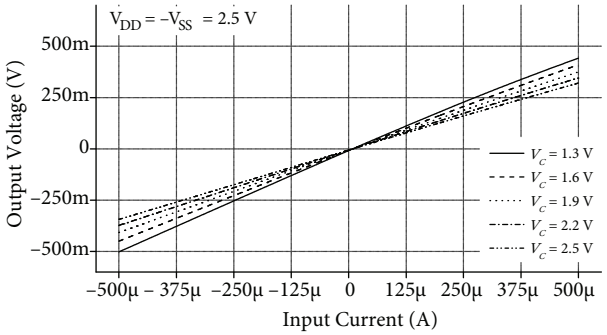

Figure 5. Output voltages against input currents with Shichman–Hodges model.

In Figures 7 and 8, frequency and time domain analyses are respectively given where $V_C = 1.25$ V is chosen. DC offset voltage in Figure 8 is found as 16.5 mV in simulations. As an example, widths of both of the NMOS transistors are changed from 5.5 μ m to 7.5 μ m by 0.25 μ m increments while keeping length constant; accordingly, the impedance and phase responses with respect to frequency are drawn in Figure 9, in which $V_C = 1.25$ V is chosen. Similarly, changes of the W parameter of the NMOS transistors and input and output signals of the GVCR in Figure 3 are drawn in Figure 10.

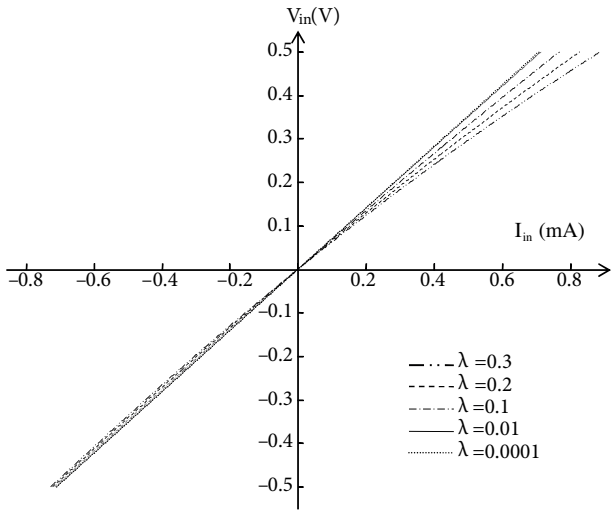

Figure 6. Output voltages against input currents by changing only the λ parameter of the MOS transistors.

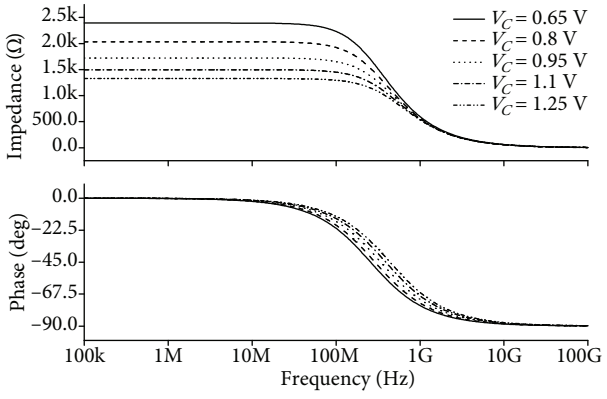

Figure 7. Impedance and phase responses of the proposed resistor against frequency.

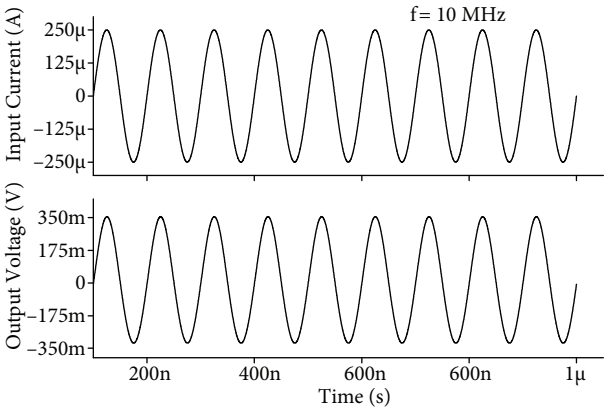

Figure 8. Input current at 10 MHz with 250 μ A peak and its corresponding output voltage where $V_C = 1.25$ V ($R_{eq} \cong 1.33$ k Ω).

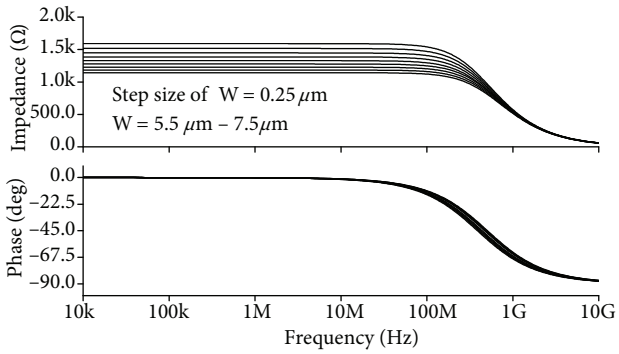

Figure 9. Impedance and phase responses for the GVCR in Figure 3 by changing only W of the NMOS transistors where $V_C = 1.25$ V ($R_{eq} \cong 1.33$ k Ω).

After fifty runs, a Monte Carlo simulation by changing 5% Gaussian variation of V_{TP} and V_{TN} parameters of all the MOS transistors is achieved as shown in Figure 11. It is seen from Figure 11 that the circuit is a bit sensitive to variation of threshold voltages.

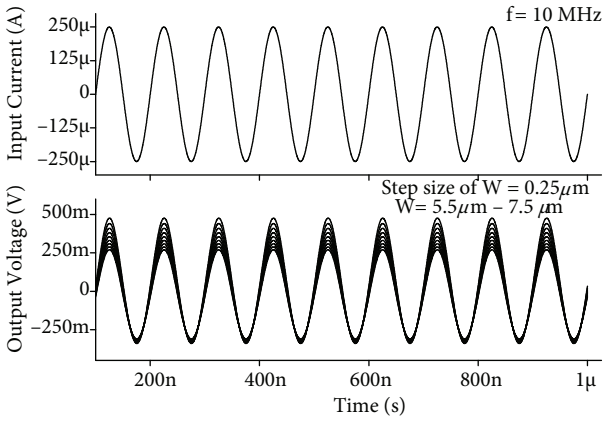

Figure 10. Input and output signals of the GVCR in Figure 3 by changing only W of the NMOS transistors where $V_C = 1.25$ V ($R_{eq} \cong 1.33$ k Ω).

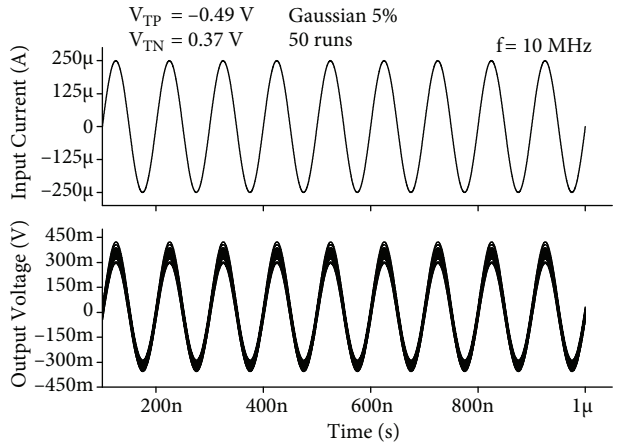

Figure 11. A Monte Carlo analysis with 5% variation of threshold voltages where $V_C = 1.25$ V ($R_{eq} \cong 1.33$ k Ω).

It is seen from simulation results in Figures 4–11 that the proposed GVCR is linear for sufficiently small input currents/voltages. The total harmonic distortion (THD) variations of the proposed GVCR versus applied peak sinusoidal input current at 10 MHz and with respect to frequency are respectively given in Figures 12 and 13, where $V_C = 1.25$ V is chosen. Additionally, in Figure 13, a sinusoidal input current with 250 μ A peak is applied. Comparison of the previously published GVCRs and the proposed one are given in Table 1.

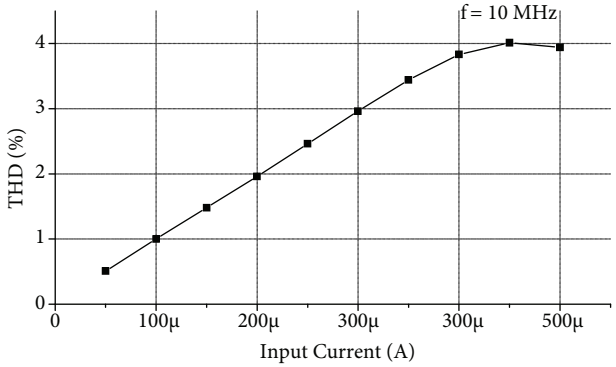

Figure 12. THD variations against peak sinusoidal input currents where V_C = 1.25 V ($R_{eq} \cong$ 1.33 k Ω).

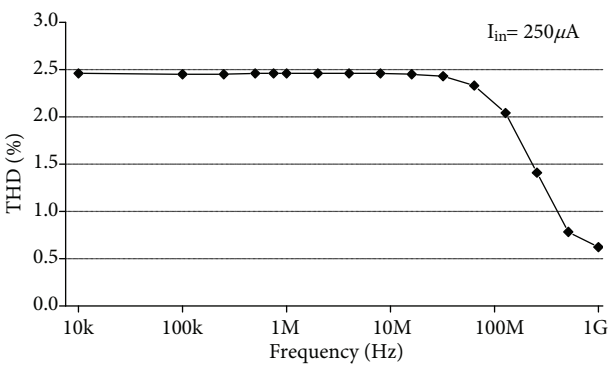

Figure 13. THD variations with respect to frequency where V_C = 1.25 V ($R_{eq} \cong$ 1.33 k Ω).

Table 1. Comparison of previously published MOS transistor-based GVCRs and the proposed one.

References	Control or particular resistor values	Number of transistors		Number of control voltage(s) or current(s)	Bias voltage(s) or current(s)	Power supplies	Power dissipation	Technology
		Linear region	Saturation region					
[1]	NA	1	4	1	0	± 5 V	NA	*
[2]	60–200 k Ω	1	8	1	1	± 5 V	NA	*
[3]	NA	0	2	2	0	± 5 V	NA	*
[4]	NA	0	4	2	0	± 5 V	NA	*
[5]	500–1600 Ω	0	8	2	0	± 1.5 V	≅ 2 mW	0.25 μ m
[6]	NA	2	1	1	0	5 V	NA	3 μ m
This work	≤ 2.39 k Ω	1	2	1	0	± 1.25 V	0.44 mW	0.25 μ m

NA: Not available. *: Old technology.

6. An application: second-order multifunctional filter

Tunable resistors are used in many circuit applications such as oscillators [32,33], filters [29,34], and inductor simulators [35–37]. As an application of the proposed GVCR, a DVCC-based second-order multifunctional filter is given. The electrical symbol of the DVCC with four terminals is depicted in Figure 14. The internal structure of the DVCC with V_B = 0.57 V is given in Figure 15 [38], where the dimensions of M_1 –M_8 (PMOS transistors) are chosen as 80 μ m / 1 μ m and the dimensions of M_9 –M_{12} (NMOS transistors) are chosen as 30 μ m / 1 μ m. The proposed filter employing two DVCCs provides low-pass (LP), high-pass (HP), and band-pass (BP) responses. It has high input impedances. All the passive elements are grounded. The circuit schematic of the

proposed filter application is given in Figure 16. Here, the proposed GVCR is replaced instead of each of all the resistors R_1, R_2, and R_3. The capacitors C_1 and C_2 are selected as 50 pF. V_C is changed from 0.65 V to 1.25 V by a step size of 150 mV.

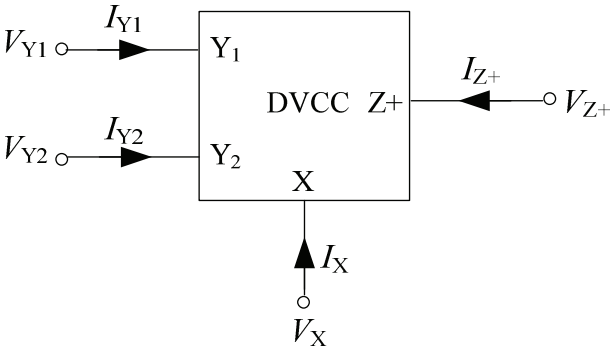

Figure 14. Electrical symbol of the DVCC.

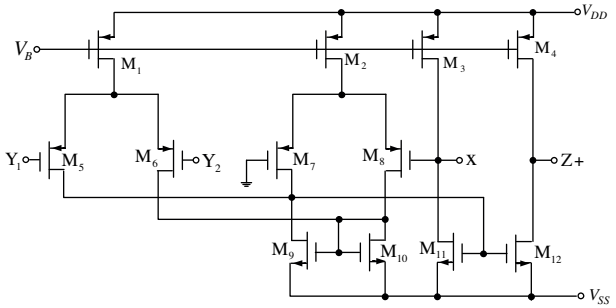

Figure 15. Internal structure of the DVCC [38].

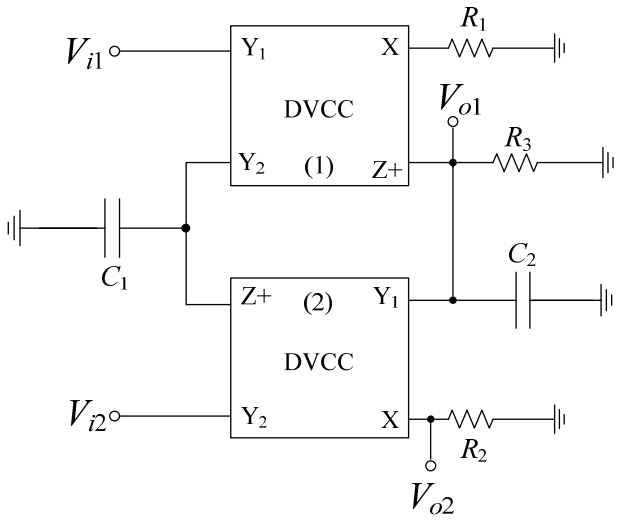

Figure 16. Proposed second-order multifunctional filter application.

The DVCC can be expressed with the following matrix equation:

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Z+} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Z+} \end{bmatrix}. \tag{18}$$

Therefore, output responses of the proposed filter in Figure 16 are found as

$$V_{o1} = \frac{R_2\left(sC_1R_3V_{i1} + V_{i2}\right)}{s^2C_1C_2R_1R_2R_3 + sC_1R_1R_3 + R_2}, \tag{19a}$$

$$V_{o2} = \frac{sC_1R_3\left(-R_2V_{i1} + R_1V_{i2} + sC_2R_1R_2V_{i2}\right)}{s^2C_1C_2R_1R_2R_3 + sC_1R_1R_3 + R_2}. \tag{19b}$$

The conditions to obtain LP, HP, and BP responses are summarized in Table 2.

Table 2. Multifunctional filter output responses.

Responses	Input terminal	Conditions	Output terminal
Low-pass	V_{i2}	$V_{i1} = 0$	V_{o1}
High-pass	$V_{i1} = V_{i2}$	$R_1 = R_2$	V_{o2}
Band-pass	V_{i1}	$V_{i2} = 0$	V_{o1}

Here, angular resonance frequency ω_o and quality factor Q are evaluated as

$$\omega_o = \sqrt{\frac{1}{C_1 C_2 R_1 R_3}}, \tag{20a}$$

$$Q = R_2 \sqrt{\frac{C_2}{C_1 R_1 R_3}}. \tag{20b}$$

LP, HP, and BP gain responses of the proposed filter application in Figure 16 are respectively shown in Figure 17.

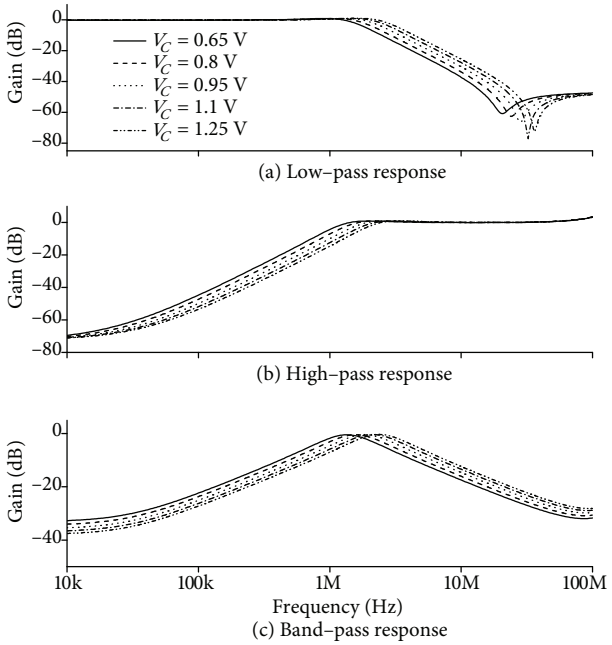

Figure 17. Gain responses of the proposed second-order multifunctional filter application.

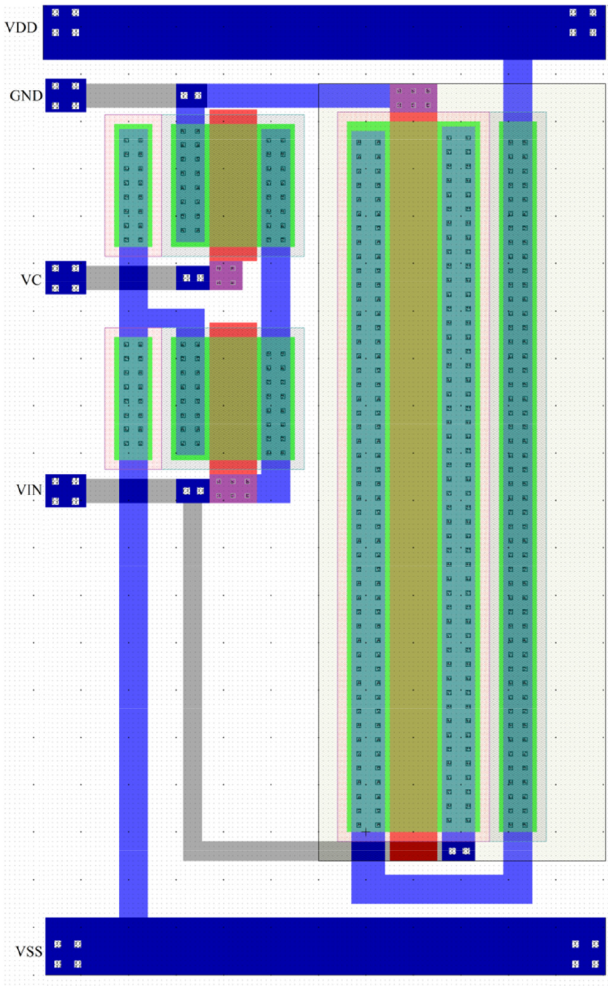

Figure 18. Layout of the proposed GVCR.

The ideal and simulation results are close to each other, whereas the difference between them can be attributed to nonidealities of the MOS transistors. The layout of the proposed GVCR is drawn in Figure 18. The layout area is about 1100 μ m^2.

7. Conclusion

The proposed wideband linear GVCR employing only three MOS transistors has a single control voltage for electronically tuning its linear resistive values in integrated circuit processes. It is seen from simulation results that the proposed tunable grounded resistor has a linear V-I relationship for suitably chosen applied input currents/voltages. The obtained postlayout simulation results with SPICE verify the claimed theory well, as expected, whereas the discrepancy between ideal and simulation results arises from nonidealities of the MOS transistors. In this study, currents are applied as inputs and voltages are measured as outputs in simulations. If voltages are applied as inputs and currents are measured as outputs, the same results can be obtained. As an application example, a new second-order multifunctional filter employing two DVCCs and only grounded passive elements is given.

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References

[1] Wang Z. Novel voltage-controlled grounded resistor. Electron Lett 1990; 26: 1711-1712.

[2] Wilson G, Chan PK. Novel voltage-controlled grounded resistor. Electron Lett 1989; 25: 1725-1726.

[3] Wang Z. 2-MOSFET transresistor with extremely low distortion for output reaching supply voltages. Electron Lett 1990; 26: 951-952.

[4] Park CS, Schaumann R. A high-frequency CMOS linear transconductance element. IEEE T Circuits Syst 1986; 33: 1132-1138.

[5] Yuce E, Minaei S, Alpaslan H. Novel CMOS technology-based linear grounded voltage controlled resistor. J Circuit Syst Comp 2011; 20: 447-455.

[6] Wang Z. Current-controlled linear MOS earthed and floating resistors and their application. IEE P-Circ Dev Syst 1990; 137: 479-481.

[7] Maloberti F. Analog Design for CMOS VLSI Systems. Boston, MA, USA: Kluwer Academic Publishers, 2001.

[8] Saaid O, Fabre A. Class AB current-controlled resistor for high performance current-mode applications. Electron Lett 1996; 32: 4-5.

[9] Arslanalp R, Yuce E, Tola, AT. Low component count BJT technology based current controlled tunable resistors and their applications. IET Circ Device Syst 2013; 7: 21-30.

[10] Maundy B, Gift S, Aronhime P. Practical voltage/current-controlled grounded resistor with dynamic range extension. IET Circ Device Syst 2008; 2: 201-206.

[11] Pandey R, Gupta M. FGMOS based voltage-controlled grounded resistor. Radioengineering 2010; 19: 455-459.

[12] Senani R, Bhaskar DR. Comment: Practical voltage/current-controlled grounded resistor with dynamic range extension. IET Circ Device Syst 2008; 2: 465-466.

[13] Senani R, Bhaskar DR. A simple configuration for realizing voltage-controlled impedances. IEEE T Circuits-I 1992; 39: 52-59.

[14] Senani R, Bhaskar DR. Realization of voltage-controlled impedances. IEEE T Circuits Syst 1991; 38: 1081-1086.

[15] Senani R, Bhaskar DR. Realization of voltage-controlled impedances. IEEE T Circuits Syst 1992; 39: 162.

[16] Senani R. Correspondence: Universal linear voltage-controlled-impedance configuration. IEE P-Circ Dev Syst 1995; 142: 208.

[17] Senani R, Bhaskar DR. Versatile voltage-controlled impedance configuration. IEE P-Circ Dev Syst 1994; 141: 414-416.

[18] Senani R. Realization of linear voltage-controlled resistance in floating form. Electron Lett 1994; 30: 1909-1911.

[19] Senani R. Floating GNIC/GNII configuration realized with only a single OMA. Electron Lett 1995; 31: 423-425.

[20] Senani R. Realization of a class of analog signal processing / signal generation circuits: novel configurations using current feedback op-amps. Frequenz 1998; 52: 196-206.

[21] Manolescu A, Popa C. Low-voltage low-power improved linearity CMOS active resistor circuits. Analog Integr Circ S 2010; 62: 373-387.

[22] Fard RA, Pooyan M. A low voltage and low power parallel electronically tunable resistor with linear and nonlinear characteristics. Microelectr J 2012; 43: 492-500.

[23] Wee KH, Sarpeshkar R. An electronically tunable linear or nonlinear MOS resistor. IEEE T Circuits-I 2008; 55: 2573-2583.

[24] Tekin SA, Ercan H, Alçı M. Novel low voltage CMOS current controlled floating resistor using differential pair. Radioengineering 2013; 22: 428-433.

[25] Kumngern M, Torteacnchai U, Dejhan K. Voltage-controlled floating resistor using DDCC. Radioengineering 2011; 20: 327-333.

[26] Metin B, Herencsar N, Cicekoglu O. A low-voltage electronically tunable MOSFET-C voltage-mode first-order all-pass filter design. Radioengineering 2013; 22: 985-994.

[27] Yuce E. Multiplier, frequency doubler and squarer circuits based on voltage controlled resistors. AEU-Int J Electron C 2011; 65: 244-249.

[28] Razavi B. Fundamentals of Microelectronics. 2nd ed. New York, NY, USA: Wiley, 2008.

[29] Yuce E, Minaei S. Universal current-mode filters and parasitic impedance effects on the filter performances. Int J Circ Theor App 2008; 36: 161-171.

[30] Shichman H, Hodges DA. Modeling and simulation of insulated-gate field-effect transistor switching circuits. IEEE J Solid-St Circ 1968; SC-3: 285-289.

[31] Razavi B. Design of Analog CMOS Integrated Circuits. 1st ed. New York, NY, USA: McGraw Hill, 2001.

[32] Herencsar N, Sotner R, Koton J, Misurec J, Vrba K. New compact VM four-phase oscillator employing only single z-copy VDTA and all grounded passive elements. Elektron Elektrotech 2013; 19: 87-90.

[33] Jerabek J, Sotner R, Vrba K. Tunable multiphase oscillator using diamond transistors with voltage controlled condition of oscillation for amplitude stabilization. Elektron Elektrotech 2014; 20: 45-48.

[34] Minaei S, Ibrahim MA. A mixed-mode KHN-biquad using DVCC and grounded passive elements suitable for direct cascading. Int J Circ Theor App 2009; 37: 793-810.

[35] Yuce E, Minaei S. Novel floating simulated inductors with wider operating-frequency ranges. Microelectr J 2009; 40: 928-938.

[36] Yuce E. On the implementation of the floating simulators employing a single active device. AEU-Int J Electron C 2007; 61: 453-458.

[37] Yuce E. On the realization of the floating simulators using only grounded passive components. Analog Integr Circ S 2006; 49: 161-166.

[38] Chiu W, Liu SI, Tsao HW, Chen JJ. CMOS differential difference current conveyors and their applications. IEE P-Circ Dev Syst 1996; 143: 91-96.