A New Electronically Fine Tunable Grounded Voltage Controlled Positive Resistor

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***Abstract*—A new grounded voltage controlled positive resistor (GVCPR) is proposed in this brief. The proposed GVCPR with a single control voltage is composed of only six MOS transistors operated in saturation region. It has the feature of fine tunability from about 770 Ω to about 1370 Ω. It can be operated properly up to a few hundreds of MHz. It has low power consumption and a wide dynamic range. It does not need any bias currents and voltages. However, its control voltage does not have the property of high input impedance and it requires some active element matching conditions. A novel second-order voltage-mode multifunction filter is given as an application example. A lot of simulation results and some experimental tests are achieved in order to verify the theory.**

***Index Terms*—MOS transistor, tunable grounded resistor, voltage-mode, multifunction filter.**

I. Introduction

IT IS a well-known fact that the direct realization of a resistor in integrated circuit (IC) process is usually undesired because it occupies large chip area. Further, it has accuracy restrictions, lack of tunability, etc. Therefore, electronically tunable active resistors [1]–[19] which can be replaced instead of resistive components of the active circuits such as analog filters, simulated inductors, oscillators, etc. to achieve external adjustability in ICs have been reported in open literature.

The grounded voltage controlled positive resistors (GVCPRs) [1]–[13], [19] which can be tuned via control voltage (V_C) are widely used. Early GVCPRs [1]–[8] employ a small number of MOS transistors. However, one or several MOS transistors of them are operated in linear region; thus, they have limited dynamic ranges (DRs). Although GVCPR in [7] dissipates very low power, it needs extra voltage sources namely, -V_{TP} and -V_{TN}. The GVCPRs in [2] and [9]–[11] have two symmetrical control voltages in opposite sign; thus, they require extra circuits. Some studies in [2]–[4] and [12] need one or more than one bias voltage; accordingly, they require additional circuits. The tunable resistor in [12] employs a number of MOS transistors; accordingly, it occupies large chip area. The GVCPRs in [13] use eight or ten MOS transistors operated in saturation region. The works in [14] use control current(s) to tune the resistivity; accordingly, they need extra MOS transistor(s). A study in [15] uses a JFET and additional active elements such as one plus-type second-generation current conveyor and a voltage buffer. The tunable resistor of [15] has been commented in [16]. The comment in [16] also deals with previously published works. The current-controlled tunable resistors in [17] and [18] employ BJTs which are temperature dependent. A floating gate MOSFET (FGMOS) based GVCPR has been reported in [19] but it has an FGMOS in linear region. On the other hand, a GVCPR can be easily obtained from an operational transconductance amplifier (OTA) whereas OTA has limitations at high frequencies.

A new GVCPR which can be tuned via a single V_C is proposed in this brief. The proposed GVCPR is made up of only six MOS transistors operated in saturation region. It has the property of fine tunability in a wide resistive range. It can be worked at high frequencies. It has low power dissipation and low total harmonic distortion (THD). However, its V_C does not have the feature of high input impedance. As an application example, a novel second-order voltage-mode (VM) multifunction filter consisting of only grounded passive components and two plus-type differential voltage current conveyors (DVCC+s) is given. It can simultaneously realize high-pass (HP), band-pass (BP) and low-pass (LP) transfer functions (TFs) without requiring any critical passive component matching conditions. A number of simulation results and several experimental tests are included in order to explain the theory.

II. The Proposed Tunable Resistor

The proposed GVCPR given in Fig. 1 uses two PMOS and four NMOS transistors operated in saturation region. PMOS transistors M_2 and M_3 with $(W/L)_2 = (W/L)_3$ ($I_{D2} = I_{D6}$) are operated as a current mirror throughout this brief in which L is the channel length and W is the channel width. Also, V_{DD} and V_{SS} are symmetrical DC power supply voltages. Drain currents of the NMOS transistors in Fig. 1, I_{D1}, I_{D4}, I_{D5} and I_{D6} are respectively found as follows:

$$I_{D1} = 0.5 \times k_{n1} \times (V_{DD} - V_{in} - V_{TNo})^2 \quad (1a)$$

$$I_{D4} = 0.5 \times k_{n4} \times (V_{in} - V_C - V_{TNo})^2 \quad (1b)$$

$$I_{D5} = 0.5 \times k_{n5} \times (-V_{SS} - V_{TNo})^2 \quad (1c)$$

$$I_{D6} = 0.5 \times k_{n6} \times (-V_C - V_{TNo})^2 \quad (1d)$$

Here, $k_{ni} = \mu_n C_{ox}(W/L)_i$ ($i = 1, 4, 5, 6$) is transconductance parameter of the ith NMOS transistor, μ_n is mobility of the NMOS transistor and C_{ox} is the gate oxide capacitance per unit area. Also, V_{TNo} is defined as threshold voltage of the NMOS transistor without considering body effect. From equations (1), input current (I_{in}) with $V_{SS} = -V_{DD}$, $k_{n1} = k_{n4} = k_{n5} = k_{n6} = k_n$ and $I_{D2} = I_{D6}$ can be computed as

$$I_{in} = -I_{D1} + I_{D4} + I_{D5} - I_{D2} = k_n V_{in}(V_{DD} - V_C - 2V_{TNo}) \quad (2)$$

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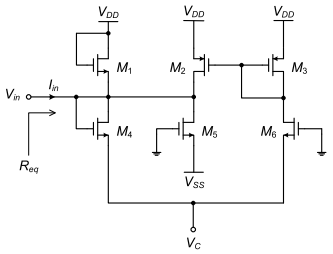

Fig. 1. The proposed grounded voltage controlled positive resistor.

From equation (2), equivalent resistance (R_{eq}) is evaluated as

$$R_{eq} = \frac{V_{in}}{I_{in}} = \frac{1}{k_n(V_{DD} - V_C - 2V_{TNo})} \tag{3}$$

As shown in equation (3), R_{eq} can be controlled via V_C. For fine operation of the proposed GVCPR, all the MOS transistors must be operated in saturation region ($V_{GS} > V_{TNo}$ and $V_{DS} > V_{GS} - V_{TNo}$ must be simultaneously satisfied for the NMOS transistors as well as $V_{SG} > |V_{TPo}|$ and $V_{SD} > V_{SG} - |V_{TPo}|$ must be simultaneously satisfied for the PMOS transistors [20]); thus, from equations (1), the following constraints must be satisfied:

$$\left.\begin{array}{c} V_{DD} - V_{TNo} > V_{in} > V_C + V_{TNo} \\ V_C < -V_{TNo} \end{array}\right\} \forall V_{in} \tag{4}$$

From equation (3), V_C sensitivity with respect to R_{eq} can be calculated as

$$S_{V_C}^{R_{eq}} = \frac{V_C}{V_{DD} - V_C - 2V_{TNo}} \tag{5}$$

Parallel parasitic capacitor (C_p) of the proposed GVCPR given in Fig. 1 can be calculated as follows:

$$C_p \cong C_{gs1} + C_{ds1} + C_{gs4} + C_{ds4} + C_{ds2} + C_{ds5} \tag{6}$$

C_p is effective at high frequencies. Input impedance (Z_{in}) of the proposed GVCPR can be written as [21]

$$Z_{in}(\omega) = \frac{V_{in}}{I_{in}} = \frac{R_{eq}}{1 + j\omega R_{eq}C_p} = \frac{R_{eq}}{1 + \frac{j\omega}{\omega_0}} \tag{7}$$

where $\omega_0 = 1/(R_{eq}C_p)$ is an angular pole frequency. For proper operation of the proposed GVCPR in Fig. 1, operating frequency $f << f_0 = \omega_0/(2\pi)$ should be chosen. In other words, $f = 0.1 \times f_0$ should be chosen for proper operation of the proposed GVCPR [22]. Also, linearity of the proposed GVCPR can be increased by the methods given in [23]. Apart from this, a PMOS transistor can be used instead of V_C in Fig. 1 to obtain high input impedance V_C as explained in [24].

III. Channel Length Modulation and Body Effects

MOS transistors which are non-linear devices have several second-order effects such as channel length modulation, body effects, etc. Only considering the channel length modulation effects with $\lambda_n = \lambda_p = \lambda$ and $k_{n1} = k_{n4} = k_{n5} = k_{n6} = k_n$ for simplicity and ignoring channel length modulation effects of the MOS transistors M_3 and M_6 for further simplicity, drain currents of the MOS transistors in Fig. 1 can be obtained as

$$I_{D1} = 0.5 \times k_n \times (V_{DD} - V_{in} - V_{TNo})^2(1 + \lambda V_{DS1}) \tag{8a}$$
$$I_{D4} = 0.5 \times k_n \times (V_{in} - V_C - V_{TNo})^2(1 + \lambda V_{DS4}) \tag{8b}$$
$$I_{D5} = 0.5 \times k_n \times (-V_{SS} - V_{TNo})^2(1 + \lambda V_{DS5}) \tag{8c}$$
$$I_{D2} = 0.5 \times k_n \times (-V_C - V_{TNo})^2(1 + \lambda V_{SD2}) \tag{8d}$$

If $V_C = V_{SS} = -V_{DD}$ and $I_{D2} = I_{D6}$ are taken into account, $I_{in} = -I_{D1} + I_{D4} + I_{D5} - I_{D2}$ can be expressed as

$$I_{in} = a_0 + a_1V_{in} + a_2V_{in}^2 + a_3V_{in}^3 \tag{9}$$

where

$$a_0 = a_2 = 0 \tag{10a}$$
$$a_1 = 2 \times k_n \times \left(2\lambda V_{DD}^2 + V_{DD}(1 - 3\lambda V_{TNo}) + \lambda V_{TNo}^2 - V_{TNo}\right) \tag{10b}$$
$$a_3 = \lambda k_n \tag{10c}$$

are obtained. It is desired that a_3 in equation (10c) must be small enough. Therefore, λ in equation (10c) can be performed as small as possible by choosing channel length of the MOS transistors of the proposed GVCPR as large as possible [20]. If only body effects are considered, R_{eq} given in equation (3) turns to

$$R_{eq} = \frac{1}{k_n \times (V_{DD} - V_C - V_{TN} - V_{TNo})} \tag{11}$$

Here, V_{TN} is expressed as in the following [20]:

$$V_{TN} = V_{TNo} + \gamma_n\left(\sqrt{|2\phi_{Fn}| + V_C - V_{SS}} - \sqrt{|2\phi_{Fn}|}\right) \tag{12}$$

Here, ϕ_{Fn} and γ_n are technology parameters. R_{eq} in equation (11) does not have non-linear terms due to body effects but values of the threshold voltages of M_4 and M_6 a bit increase.

IV. Mismatch Analyses

It is assumed that $V_{SS} = -V_{DD}, k_{n1} = k_n + \Delta k_n, k_{n4} = k_{n5} = k_{n6} = k_n$ and $I_{D2} = I_{D6}$ in Fig. 1, I_{in} can be evaluated as

$$\begin{aligned} I_{in} &= -I_{D1} + I_{D4} + I_{D5} - I_{D2} \\ &= V_{in}(k_n(V_{DD} - V_C - 2V_{TNo}) + (V_{DD} - V_{TNo})\Delta k_n) \\ &\quad + \left(V_{DD}(V_{TNo} - 0.5V_{DD}) - 0.5V_{TNo}^2\right)\Delta k_n - 0.5V_{in}^2\Delta k_n \end{aligned} \tag{13}$$

Here, Δk_n is an undesired variation of the parameter k_n of M_1 transistor. It is observed from equation (13) that due to Δk_n, I_{in} has an unwanted non-linear term which is evaluated as $-0.5V_{in}^2\Delta k_n$ and an undesired DC term which is found as $(V_{DD}(V_{TNo} - 0.5V_{DD}) - 0.5V_{TNo}^2)\Delta k_n$. Also, due to non-linear term in equation (13), V_{in} should be chosen as [22]

$$|V_{in}| \leq \frac{1}{10} \times \frac{k_n(V_{DD} - V_C - 2V_{TNo}) + (V_{DD} - V_{TNo})\Delta k_n}{0.5 \times \Delta k_n} \tag{14}$$

For an example, if threshold voltage values of all the NMOS transistors in Fig. 1 except M_1 are V_{TNo} and threshold voltage value of M_1 is V_{TN}, I_{in} in Fig. 1 can be computed as

$$\begin{aligned} I_{in} &= -I_{D1} + I_{D4} + I_{D5} - I_{D2} \\ &= k_n \times (V_{DD} - V_C - V_{TN} - V_{TNo})V_{in} \\ &\quad + 0.5 \times k_n \times \left(2V_{DD}(V_{TN} - V_{TNo}) + V_{TNo}^2 - V_{TN}^2\right) \end{aligned} \tag{15}$$

It is seen from equation (15) that I_{in} has an undesired DC term due to threshold voltage mismatch. Also, undesired DC term is found as $0.5 \times k_n \times (2V_{DD}(V_{TN} - V_{TNo}) + V_{TNo}^2 - V_{TN}^2)$.

V. Simulation Results

The proposed GVCPR is simulated by using 0.25μm TSMC CMOS technology parameters given in [25]. Symmetrical DC power supply voltages of the proposed GVCPR in Fig. 1 are chosen as $V_{DD} = -V_{SS} = 1.25$V. Dimensions of the NMOS and PMOS transistors are chosen as 5μm / 1μm and 15μm / 1μm, respectively. Bulks of all the MOS transistors are connected to their relevant sources.

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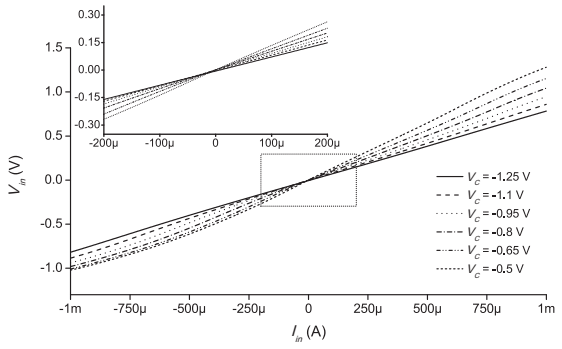

Fig. 2. DC characteristics of the proposed GVCPR.

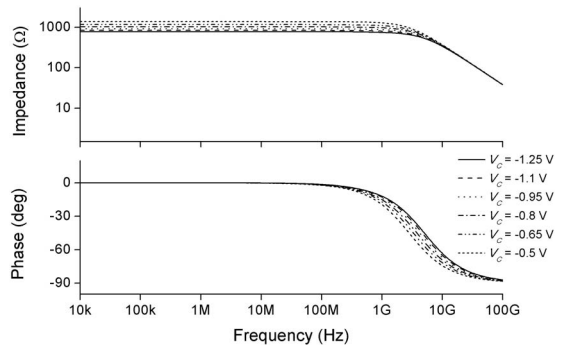

Fig. 3. Impedance and phase response of the proposed GVCPR.

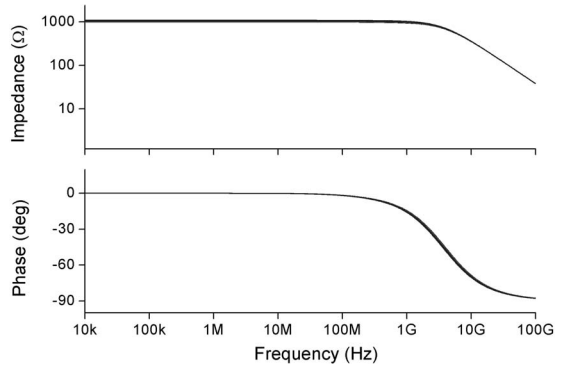

Fig. 4. A Monte Carlo frequency domain analysis of the proposed GVCPR with 2% Gaussian variations of the threshold voltages where $V_C = -0.8$V.

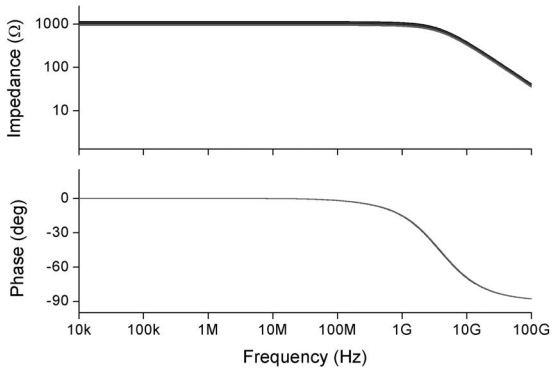

Fig. 5. Impedance and phase responses of the proposed GVCPR by changing only widths of the NMOS transistors where $V_C = -0.8$V is chosen.

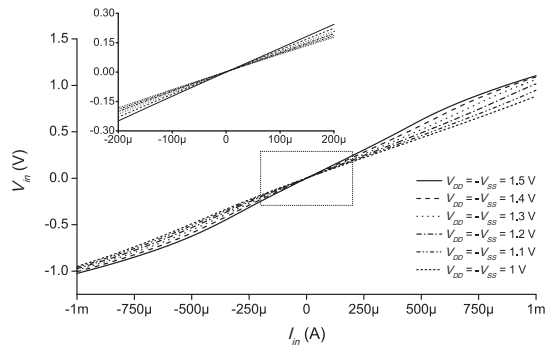

Fig. 6. Input current and voltage characteristics of the proposed GVCPR obtained by varying DC power supply voltages from ±1 V to ±1.5 V.

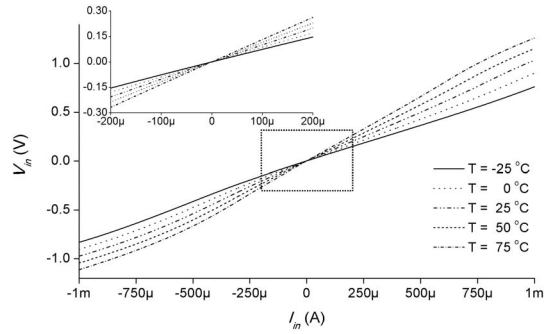

Fig. 7. Input current and voltage characteristics of the proposed GVCPR obtained by varying temperature values from -25 °C to 75 °C.

DC characteristics of the proposed GVCPR are drawn in Fig. 2 in which I_{in} is changed from -1mA to 1mA. Further, V_C is varied from -1.25 V ($R_{eq} \cong 770\ \Omega$ and total power dissipation is found as 2.15 mW in SPICE simulation) to -0.5V ($R_{eq} \cong 1370\ \Omega$ and total power dissipation is found as 0.74 mW in SPICE simulation) by an increment of 0.15V. It is seen from Fig. 2 that V-I characteristics of the proposed GVCPR are sufficiently linear. Furthermore, if $V_C = -0.4$V and $V_{DD} = -V_{SS} = 0.45$V are chosen, $R_{eq} \cong 17\ \text{k}\Omega$ and total power consumption is found as 3.18 μW in SPICE simulation.

Impedance and phase responses of the GVCPR in Fig. 1 are shown in Fig. 3 but if real features of IC are considered, bandwidth of the GVCPR in Fig. 1 will decrease considerably. After fifty runs, a Monte Carlo analysis by changing 2% Gaussian variation of V_{THo} parameters of all the MOS transistors is achieved to obtain frequency domain responses of the proposed GVCPR in which $V_C = -0.8$V is chosen, which is demonstrated in Fig. 4. As an example, widths of all of the NMOS transistors are changed from 4.5μm to 5.5μm by an increment of 0.25μm while keeping length constant; accordingly, the impedance and phase responses with respect to frequency are drawn in Fig. 5 where $V_C = -0.8$V is chosen. If symmetrical DC power supply voltages are changed from ±1V to ±1.5V by a step size of 0.1V, noticeable variations are not observed in DC transfer characteristics of the proposed GVCPR as demonstrated in Fig. 6. A temperature analysis as given in Fig. 7 is performed in which the temperature is changed from -25°C to 75°C by a step size of 25°C. It is observed from Fig. 7 that equivalent resistance increases and linearity decreases while the temperature rises. For simulations in Figs. 6 and 7, V_C is selected as -0.8V. THD changes against peak amplitude of the applied sinusoidal input signal at 10 MHz are shown in Fig. 8 where $V_C = -0.8$V ($R_{eq} \cong 1000\ \Omega$ and total power dissipation is found as 1.01 mW in SPICE simulation) is chosen. It is clear from the results of the SPICE simulation shown in Fig. 8 that THD changes are smaller than 2.5% if I_{in} is changed from about 2pA which is minimum allowable input current to about 400μA which is maximum allowable input current. Therefore,

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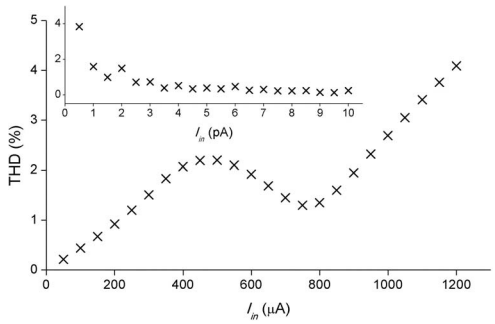

Fig. 8. THD variations of the proposed GVCPR at 10 MHz.

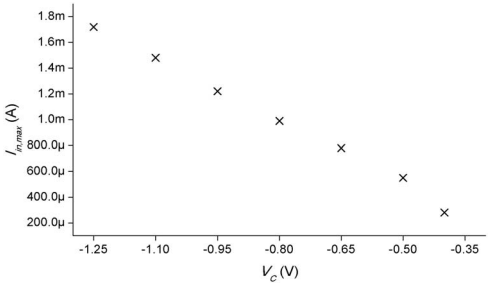

Fig. 9. Maximum allowable input currents versus control voltages at 10 MHz.

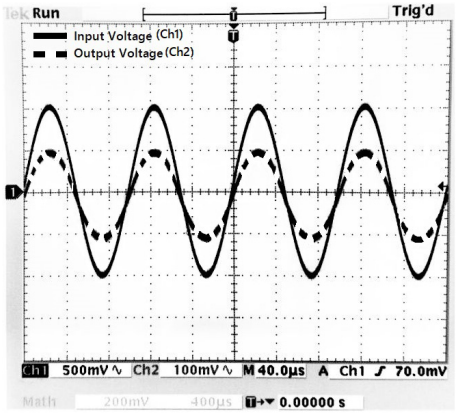

Fig. 10. Input voltage and the corresponding output voltage signals.

DR is approximately calculated as 166dB. Maximum allowable input currents with respect to V_C at 10 MHz are drawn in Fig. 9. Further, minimum allowable input currents found in SPICE simulations are very low (a few pA). It is seen from Fig. 9 that maximum allowable input currents rise while V_C decreases.

VI. Experimental Test Results

The proposed GVCPR in Fig. 1 is implemented on a breadboard by using commercially available discreet NMOS and PMOS transistors which are called as 2N7000 ($V_{TH} \cong 0.8$ V) and BS250 ($V_{TH} \cong -1.9$ V), respectively. Additionally, only one AD844 and a resistor (R) with 1 kΩ value connected to the X terminal of the AD844 are used to generate input current($I_{in} = V_{in}/R$) from the Z terminal of the AD844. A sinusoidal input voltage (V_{in}) with 1 V peak at 10 kHz is applied to the Y terminal of the AD844; thus, I_{in} of the proposed GVCPR is obtained as 1 mA peak. V_{in} and the corresponding output voltage ($R_{eq} \times I_{in}$) are obtained as shown in Fig. 10 in which R_{eq} is approximately found as 100 Ω (total power consumption is approximately evaluated as 134 mW in experimental test). The symmetrical DC power supply voltages in experimental test are chosen as ±2.1 V while V_C is chosen as -2.1 V. Simulation and experimental test results of R_{eq} variations for various control voltages versus frequency are shown in Fig. 11 where simulation results corroborate experimental test results.

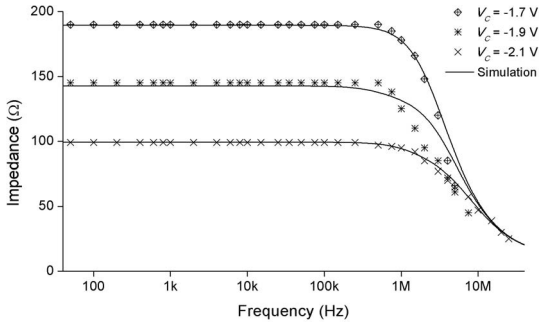

Fig. 11. Equivalent resistance variations for various control voltages with respect to frequency.

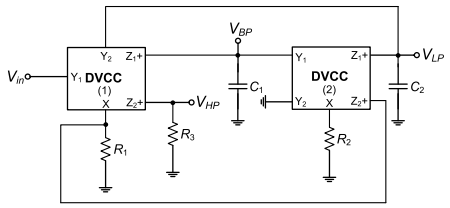

Fig. 12. The proposed second-order voltage-mode multifunction filter.

The claimed theory is confirmed by the simulation results and experimental tests well. Nevertheless, the slight difference among ideal, simulation and experimental test results arises from non-idealities of the MOS transistors. Moreover, parasitics of the board affect the performance of the GVCPR in the experimental tests.

VII. An Application Example

VM analog filters [26]–[31] find wide application areas such as touch-tone telephone decoders, phase-locked loop FM stereo demodulators, three-way high fidelity loudspeakers, etc. As an application example, a novel second-order VM filter employing only grounded passive components is given in Fig. 12. Also, the proposed multifunction filter in Fig. 12 with high input impedance has only two DVCC+s. It can simultaneously provide the following HP, BP and LP filter TFs:

$$\frac{V_{HP}}{V_{in}} = \frac{R_3}{R_1}\frac{s^2C_1C_2R_1R_2}{s^2C_1C_2R_1R_2 + sC_2R_1 + 1} \tag{16a}$$

$$\frac{V_{BP}}{V_{in}} = \frac{R_2}{R_1}\frac{sC_2R_1}{s^2C_1C_2R_1R_2 + sC_2R_1 + 1} \tag{16b}$$

$$\frac{V_{LP}}{V_{in}} = \frac{1}{s^2C_1C_2R_1R_2 + sC_2R_1 + 1} \tag{16c}$$

From equations (16), angular resonance frequency (ω_o) and quality factor (Q) are respectively evaluated as

$$\omega_o = \frac{1}{\sqrt{C_1C_2R_1R_2}} \tag{17a}$$

$$Q = \sqrt{\frac{C_1R_2}{C_2R_1}} \tag{17b}$$

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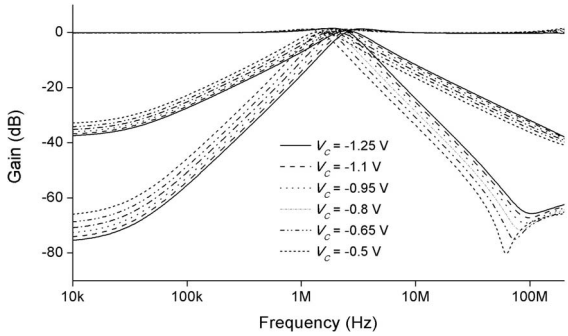

Fig. 13. Low-pass, band-pass and high-pass transfer functions.

The VM filter application in Fig. 12 with $C_1 = C_2 = 80$ pF is simulated by SPICE program. All the three resistors of it are removed and the proposed GVCPR is replaced instead of each resistor of the filter in Fig. 12. Each V_C of the proposed GVCPR is simultaneously varied from -1.25V to -0.5V by an increment of 0.15V. HP, BP and LP TFs for the VM multifunction biquadratic filter in Fig. 12 are shown in Fig. 13. Apart from this, MOS transistor based internal structure of the DVCC+ in [32] is used in the simulation of the filter in Fig. 12. Dimensions of all the NMOS and PMOS transistors in [32] are chosen as 13μm/0.5μm and 41.5μm/0.5μm, respectively. V_B is chosen as 0.5 V and $V_{DD} = 1.25$ V and $V_{SS} = -1.25$ V are chosen.

VIII. Conclusion

In this brief, a new GVCPR with a single V_C is proposed. The proposed GVCPR has the following important seven features simultaneously when compared to previously published works: **i.** it is composed of only six MOS transistors operated in saturation region, **ii.** it has the property of fine tunability from about 770 Ω to about 1370 Ω, **iii.** it can be operated up to a few hundreds of MHz, **iv.** it does not require any bias currents and voltages, **v.** it has low power dissipation, **vi.** it has a wide dynamic range and **vii.** it can be tuned up to 17 kΩ. A novel second-order VM multifunction filter made up of only grounded passive elements and two DVCC+s is given as an application example. The proposed filter application possesses the property of high input impedance resulting in easy cascadability with other VM circuits. It can simultaneously provide HP, BP and LP TFs. Also, it does not need any critical passive component matching conditions and cancellation constraints. It is expected that both of the proposed GVCPR and VM biquad will be beneficial in a number of areas such as telecommunication, signal processing, control engineering, instrumentation and measurement.

References

[1] I. S. Han and S. B. Park, "Voltage-controlled linear resistor by two MOS transistors and its application to active RC filter MOS integration," *Proc. IEEE*, vol. 72, no. 11, pp. 1655–1657, Nov. 1984.

[2] H. Youssef, R. Newcomb, and M. Zaghloul, "A CMOS voltage-controlled linear resistor with wide dynamic range," in *Proc. 21st Southeastern Symp. Syst. Theory*, Tallahassee, FL, USA, 1989, pp. 681–683.

[3] G. Wilson and P. K. Chan, "Novel voltage-controlled grounded resistor," *Electron. Lett.*, vol. 25, no. 25, pp. 1725–1726, Dec. 1989.

[4] G. Moon, M. E. Zaghloul, and R. W. Newcomb, "An enhancement-mode MOS voltage-controlled linear resistor with large dynamic range," *IEEE Trans. Circuits Syst.*, vol. 37, no. 10, pp. 1284–1288, Oct. 1990.

[5] Z. Wang, "Novel voltage-controlled grounded resistor," *Electron. Lett.*, vol. 26, no. 20, pp. 1711–1712, Sep. 1990.

[6] K. M. Al-Ruwaihi and J. M. Noras, "A novel linear resistor utilizing MOS transistors with identical sizes and one controlling voltage," *Int. J. Electron.*, vol. 76, no. 6, pp. 1083–1098, 1994.

[7] E. Yuce, S. Minaei, and N. Herencsar, "Grounded voltage controlled positive resistor with ultra low power consumption," *Elektronika Ir Elektrotechnika*, vol. 20, no. 7, pp. 45–50, 2014.

[8] E. Yuce, S. Tokat, and F. Yucel, "A new wideband electronically tunable grounded resistor employing only three MOS transistors," *Turk. J. Elect. Eng. Comput. Sci.*, vol. 24, no. 4, pp. 2442–2453, 2016.

[9] C.-S. Park and R. Schaumann, "A high-frequency CMOS linear transconductance element," *IEEE Trans. Circuits Syst.*, vol. CAS-33, no. 11, pp. 1132–1138, Nov. 1986.

[10] Z. Wang, "2-MOSFET transresistor with extremely low distortion for output reaching supply voltages," *Electron. Lett.*, vol. 26, no. 13, pp. 951–952, Jun. 1990.

[11] E. Yuce, S. Minaei, and H. Alpaslan, "Novel CMOS technology-based linear grounded voltage controlled resistor," *J. Circuits Syst. Comput.*, vol. 20, no. 3, pp. 447–455, 2011.

[12] K. H. Wee and R. Sarpeshkar, "An electronically tunable linear or non-linear MOS resistor," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 9, pp. 2573–2583, Oct. 2008.

[13] E. Yuce, S. Minaei, and H. Alpaslan, "Single voltage controlled CMOS grounded resistors and their application to video filter," *Indian J. Eng. Mater. Sci.*, vol. 21, pp. 501–509, Oct. 2014.

[14] Z. Wang, "Current-controlled linear MOS earthed and floating resistors and their application," *IEE Proc. G Circuits Devices Syst.*, vol. 137, no. 6, pp. 479–481, Dec. 1990.

[15] B. Maundy, S. Gift, and P. Aronhime, "Practical voltage/current-controlled grounded resistor with dynamic range extension," *IET Circuits Devices Syst.*, vol. 2, no. 2, pp. 201–206, Apr. 2008.

[16] R. Senani and D. R. Bhaskar, "Comment: Practical voltage/current-controlled grounded resistor with dynamic range extension," *IET Circuits Devices Syst.*, vol. 2, no. 5, pp. 465–466, Oct. 2008.

[17] O. Saaid and A. Fabre, "Class AB current-controlled resistor for high performance current-mode applications," *Electron. Lett.*, vol. 32, no. 1, pp. 4–5, Jan. 1996.

[18] R. Arslanalp, E. Yuce, and A. T. Tola, "Low-component count BJT technology-based current controlled tunable resistors and their applications," *IET Circuits Devices Syst.*, vol. 7, no. 1, pp. 21–30, Jan. 2013.

[19] R. Pandey and M. Gupta, "FGMOS based voltage-controlled grounded resistor," *Radioengineering*, vol. 19, no. 3, pp. 455–459, 2010.

[20] B. Razavi, *Fundamentals of Microelectronics*, 2nd ed. Hoboken, NJ, USA: Wiley, 2008.

[21] E. Yuce, "Multiplier, frequency doubler and squarer circuits based on voltage controlled resistors," *AEÜ Int. J. Electron. Commun.*, vol. 65, no. 3, pp. 244–249, 2011.

[22] E. Yuce and S. Minaei, "Universal current-mode filters and parasitic impedance effects on the filter performances," *Int. J. Circuit Theory Appl.*, vol. 36, no. 2, pp. 161–171, 2008.

[23] R. Sotner *et al.*, "An additional approach to model current followers and amplifiers with electronically controllable parameters from commercially available ICs," *Meas. Sci. Rev.*, vol. 12, no. 6, pp. 255–265, 2012.

[24] F. Yucel and E. Yuce, "New highly linear tunable transconductor circuits with low number of MOS transistors," *Int. J. Electron.*, vol. 103, no. 8, pp. 1301–1317, 2016.

[25] E. Yuce, S. Minaei, and O. Cicekoglu, "Full-wave rectifier realization using only two CCII+s and NMOS transistors," *Int. J. Electron.*, vol. 93, no. 8, pp. 533–541, 2006.

[26] I. Myderrizi, S. Minaei, and E. Yuce, "An electronically fine-tunable multi-input–single-output universal filter," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 58, no. 6, pp. 356–360, Jun. 2011.

[27] V. K. Singh, A. K. Singh, D. R. Bhaskar, and R. Senani, "New universal biquads employing CFOAs," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 11, pp. 1299–1303, Nov. 2006.

[28] W.-Y. Chiu and J.-W. Horng, "High-input and low-output impedance voltage-mode universal biquadratic filter using DDCCs," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 8, pp. 649–652, Aug. 2007.

[29] C.-M. Chang, "Multifunction biquadratic filters using current conveyors," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 44, no. 11, pp. 956–958, Nov. 1997.

[30] J.-W. Horng, "High-input impedance voltage-mode universal biquadratic filter using three plus-type CCIIs," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 48, no. 10, pp. 996–997, Oct. 2001.

[31] C.-M. Chang, "New multifunction OTA-C biquads," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 46, no. 6, pp. 820–824, Jun. 1999.

[32] A. Abaci and E. Yuce, "A new DVCC+ based second-order current-mode universal filter consisting of only grounded capacitors," *J. Circuits Syst. Comput.*, vol. 26, no. 9, p. 18, 2017.

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