Turkish Journal of Electrical Engineering and Computer Sciences

Volume 24 | Number 4 Article 87

1-1-2016

A new electronically tunable first-order all-pass filter using only three NMOS transistors and a capacitor

FIRAT YÜCEL

ERKAN YUCE

Follow this and additional works at: https://journals.tubitak.gov.tr/elektrik

 Part of the Computer Engineering Commons, Computer Sciences Commons, and the Electrical and Computer Engineering Commons

Recommended Citation

YÜCEL, FIRAT and YUCE, ERKAN (2016) "A new electronically tunable first-order all-pass filter using only three NMOS transistors and a capacitor," *Turkish Journal of Electrical Engineering and Computer Sciences*: Vol. 24: No. 4, Article 87. https://doi.org/10.3906/elk-1410-95
Available at: https://journals.tubitak.gov.tr/elektrik/vol24/iss4/87

This Article is brought to you for free and open access by TÜBİTAK Academic Journals. It has been accepted for inclusion in Turkish Journal of Electrical Engineering and Computer Sciences by an authorized editor of TÜBİTAK Academic Journals. For more information, please contact academic.publications@tubitak.gov.tr.

Turkish Journal of Electrical Engineering & Computer Sciences

http://journals.tubitak.gov.tr/elektrik/

Research Article

Turk J Elec Eng & Comp Sci
(2016) 24: 3286 – 3292
© TÜBİTAK
doi:10.3906/elk-1410-95

A new electronically tunable first-order all-pass filter using only three NMOS transistors and a capacitor

Fırat YÜCEL[1,*], **Erkan YÜCE**[2]

[1]Department of Informatics, Akdeniz University, Antalya, Turkey

[2]Department of Electrical and Electronics Engineering, Pamukkale University, Denizli, Turkey

Received: 17.10.2014 • **Accepted/Published Online:** 04.04.2015 • **Final Version:** 15.04.2016

Abstract: In this paper, a new first-order voltage-mode (VM) all-pass filter that consists of only three NMOS transistors and a capacitor is proposed. The resonance frequency of the proposed circuit can be tuned electronically by a control current. It has high input impedance; thus, it can be easily cascaded with other VM circuits. Furthermore, it does not require any critical passive component matching conditions. Nevertheless, it does not have low output impedance. Although a floating capacitor is used in the proposed circuit, it can be easily realized with today's technologies. Ideal and nonideality analyses are performed for the proposed circuit. The behavior of the filter is verified by a number of SPICE simulations and an experimental test. The total harmonic distortion variations of the proposed circuit are found low enough.

Key words: All-pass filter, voltage-mode, NMOS

1. Introduction

All-pass filters (APFs) are widely used in a number of analog signal processing applications to provide phase linearity, phase shifting, signal delay processes, etc. APFs can be classified according to their operating mode such as voltage mode (VM) and current mode (CM). Some VM APFs are composed of MOS transistors [1–8]. A CM APF employs a number of MOS transistors [9]. On the other hand, the VM APFs in [10–15] contain active building blocks using tens of MOS transistors. The circuits implemented by a reduced number of transistors are given in [5,6], but they include several passive elements. The main property of VM filters is their cascadability, and thus they should have the property of high input impedance [3,7,10–14]. APFs can be tuned electronically as given in [2–4,7,8]. However, some APFs require bias voltage(s) [1,2,5,9]. The APF in [7] has high input impedance and it uses five NMOS transistors. The APF circuits in [8,9] consist of only one passive element, but they respectively contain six and seven MOS transistors. The circuit in [8] does not have high input impedance. The gains of the APFs in [2,6] are less than unity.

In the present work, a novel VM first-order APF employing only three NMOS transistors and a capacitor is proposed. The pole frequency of the proposed APF can be adjusted by changing the value of the control current. One of the main properties of the proposed APF is its high input impedances; thus, it can be easily cascaded with other VM circuits. Moreover, it does not need any critical passive element matching constraints. However, it does not have low output impedance. It consists of a floating capacitor, which can be easily realized

*Correspondence: fyucel@akdeniz.edu.tr

with today's IC technologies [16]. A number of time domain and frequency domain simulations and experimental test results are included to verify the claimed theory.

The paper is organized as follows: after the introduction in Section 1, the proposed APF structure is treated in Section 2; simulation results for the proposed APF circuit are given in Section 3; in Section 4 experimental test results are provided; and some conclusive remarks are drawn in Section 5.

2. The proposed NMOS-based APF

The proposed first-order VM APF circuit is shown in Figure 1. It consists of only three NMOS transistors, $M_1 - M_3$, one capacitor, and a control current, I_o. the M_1 and M_3 transistors behave like a unity gain inverting amplifier [7]. Thus, the drain voltage of M_3 transistor $V_{D3} = -V_{in}$. For the circuit in Figure 1, the equation can be ideally written as:

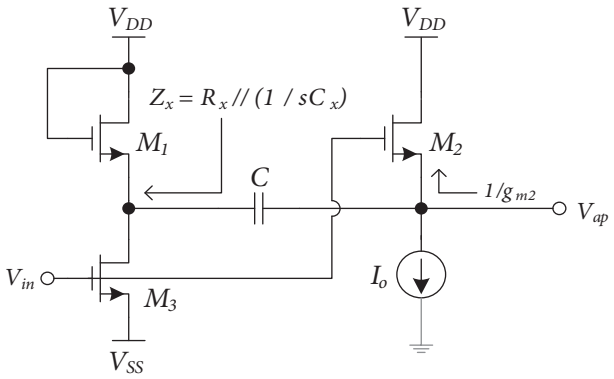

Figure 1. Proposed APF circuit.

$$(V_{in} - V_{ap})\, g_{M_2} = (V_{ap} - (-V_{in}))\, sC \tag{1}$$

where g_{M2} is the conductance of M_2 and is defined as:

$$g_{M_2} = \sqrt{2k_{n_2} I_o} \tag{2}$$

Here, $k_n = \mu_n C_{ox}(W/L)_2$ is the transconductance parameter of the NMOS transistor, μ_n is the mobility of the NMOS transistor, C_{ox} is the gate oxide capacitance per unit area, W is the channel width, and L is the channel length.

From Eq. (1), the transfer function (TF) of the proposed APF is found as:

$$\frac{V_{ap}}{V_{in}} = \frac{1 - \frac{sC}{g_{M_2}}}{1 + \frac{sC}{g_{M_2}}} \tag{3}$$

which provides noninverting first-order all-pass responses with $\omega_o = g_{M2} \;/\; C$. The phase response is evaluated as follows:

$$\phi(\omega) = -2\tan^{-1}\left(\frac{\omega C}{g_{M_2}}\right) \tag{4}$$

where the phase changes from 0^{circ} to -180^{circ} as the frequency varies from zero to infinity. Parasitic impedance Z_x can be defined as:

$$Z_x = R_x \left\| \frac{1}{sC_x} \right. \tag{5}$$

Here, R_x and C_x are respectively parasitic resistor and capacitor, which are computed as follows:

$$R_x = \frac{1}{g_{M_1}} \| r_{o1} \| r_{o3} \tag{6}$$

$$C_x \cong C_{gs1} + C_{ds1} + C_{gd3} + C_{ds3} \tag{7}$$

TF of the proposed APF with parasitic impedances is obtained as:

$$\frac{V_{ap}}{V_{in}} = \frac{g_{M_2} - \frac{sC(1+sC_xR_x)}{1+s(C+C_x)R_x}}{g_{M_2} + \frac{sC(1+sC_xR_x)}{1+s(C+C_x)R_x}} \tag{8}$$

From Eq. (8), for proper operation of the first proposed APF, the following constrains should be satisfied:

$$\omega C_x R_x << 1 \tag{9}$$

$$\omega (C + C_x) R_x << 1 \tag{10}$$

From Eq. (8), the following useful operating frequency range is obtained:

$$f \leq \frac{0.1}{2\pi} \frac{1}{(C + C_x)R_x} \tag{11}$$

It is important to note that $1 \,/\, g_{M2} << r_{o2}$ should be chosen for proper operation of the proposed APF, which can be achieved by choosing a larger length of the M_2 transistor [17].

3. Simulation results

The proposed APF is simulated by using 0.13 mu m IBM CMOS technology parameters in SPICE program. DC symmetrical power supply voltages are chosen as $V_{DD} = -V_{SS} = 0.75$ V. All the bulks of the NMOS transistors are connected to relevant sources. Dimensions of the NMOS transistors are given in Table 1. We prefer 0.13 mu m deep submicron technology because of its low power dissipation and DC symmetrical power supply voltages.

Table 1. Dimensions of the NMOS transistors.

Transistor name	Aspect ratio (W/L)
M_1 and M_3	130/0.52 mu m
M_2	1.3/0.52 mu m

In simulations, R_x in Figure 1 is calculated as 25.54 Ω and C_x is found as 416 fF. The gain and phase responses of the proposed APF with I_o variations are depicted in Figure 2, where $C = 10$ pF is selected. The gain response of the proposed APF is approximately equal to –1 dB, which is acceptable.

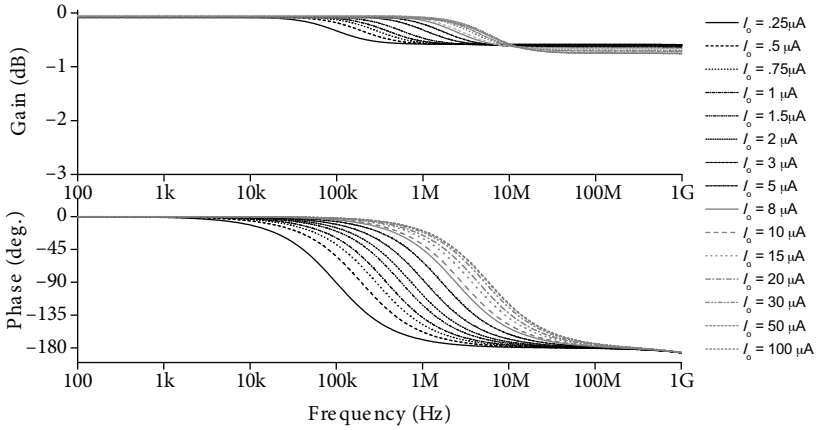

Figure 2. The gain and phase response of the proposed APF circuit.

The control current I_o is selected as 100 mu A for all simulations below and $C = 10$ pF is selected, which yields a pole frequency of 5.52 MHz. A sinusoidal input signal with a peak value of 10 mV at a frequency of 5.52 MHz is applied to show the time domain performance of the proposed APF. The input and corresponding output are given in Figure 3, where a phase difference of about 90^{circ} between the input and output signals at pole frequency is seen.

The gain and phase responses of the proposed APF circuit are given in Figure 4, where only the width of the M_2 transistor in Figure 1 is varied between 1.04 mu m and 1.56 mu m by a step size of 0.13 mu m. Additionally, a sinusoidal input signal with a peak value of 10 mV at 5.52 MHz is applied. The input and corresponding output voltages of the proposed APF circuit are drawn in Figure 5, in which only the width of the M_2 transistor in Figure 1 is varied between 1.04 mu m and 1.56 mu m by a step size of 0.13 mu m. By varying the M_2 transistor width, the change in gain is slight and offset voltages occur.

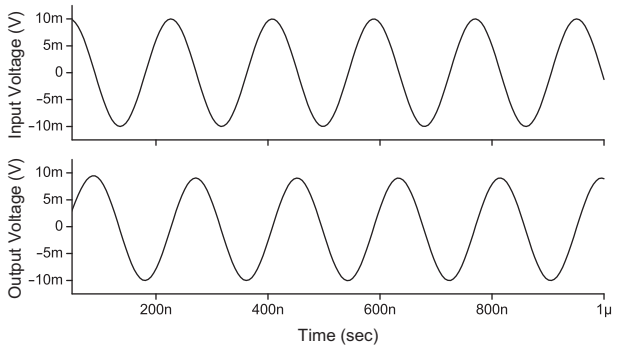

Figure 3. Input and corresponding output of the proposed APF at a frequency of 5.52 MHz.

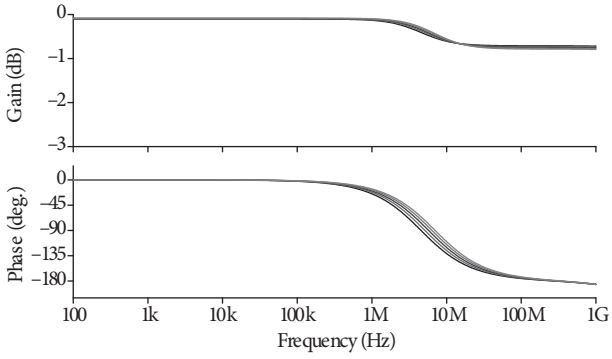

Figure 4. The gain and phase response of the proposed APF by changing W of transistor M_2.

A Monte Carlo analysis with twenty runs with 5% variations of the V_{TH0} is performed by applying a sinusoidal input signal with a peak value of 10 mV at 5.52 MHz. The result is shown in Figure 6. In this analysis, it is seen that offset voltages occur when the V_{TH0} value is changed.

To show the frequency domain and time domain responses of the proposed APF, Monte Carlo analyses with twenty runs for 20% variations of the capacitor C are given in Figures 7 and 8, respectively. The input and output noises of the proposed APF circuit are shown in Figure 9, which are adequately low values. The

total harmonic distortion (THD) variations with respect to the peak value of the applied sinusoidal signal at a frequency of 5.52 MHz are depicted in Figure 10, where it can be seen that THD variations are smaller than 1%.

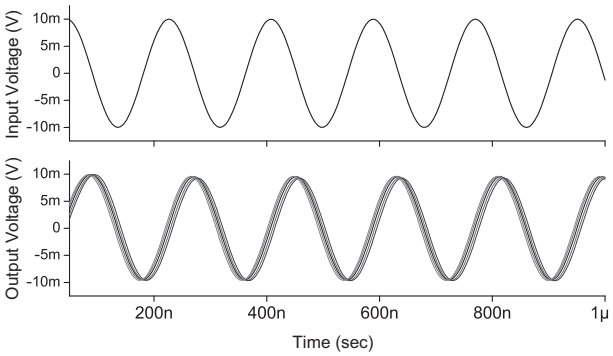

Figure 5. Input and corresponding output of the proposed APF by changing W of transistor M_2.

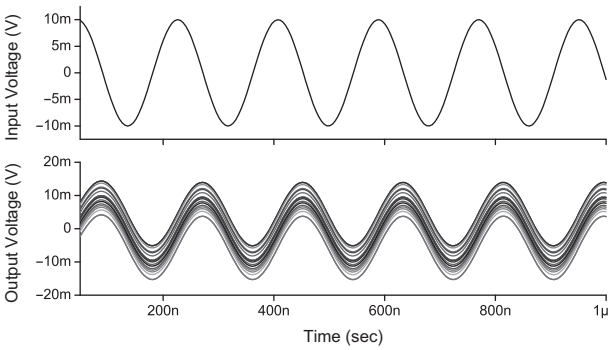

Figure 6. Monte Carlo analysis of the proposed APF circuit by changing the V_{TH0} value.

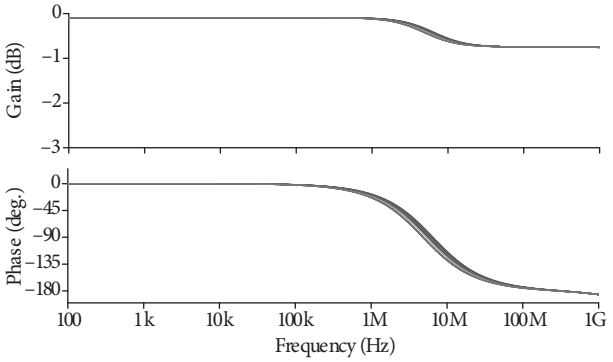

Figure 7. Monte Carlo analysis of the proposed APF circuit in the frequency domain by changing the C value.

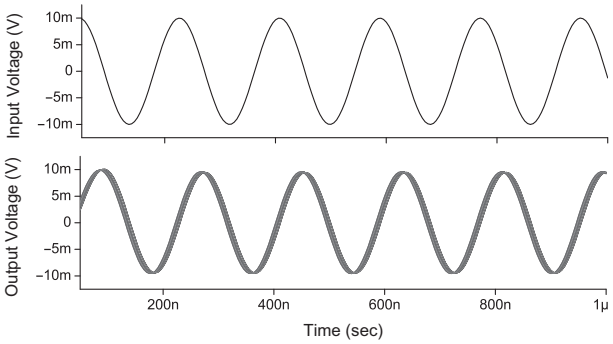

Figure 8. Monte Carlo analysis of the proposed APF circuit in the time domain by changing the C value.

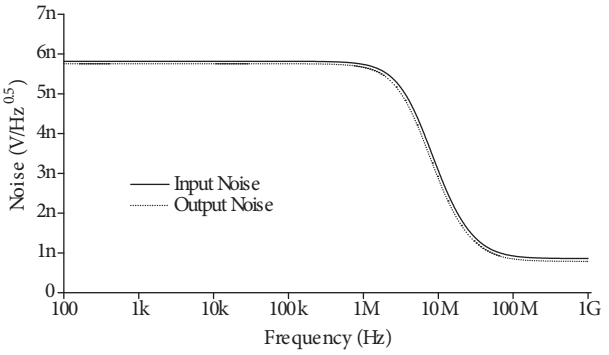

Figure 9. The input and output noises of the proposed APF.

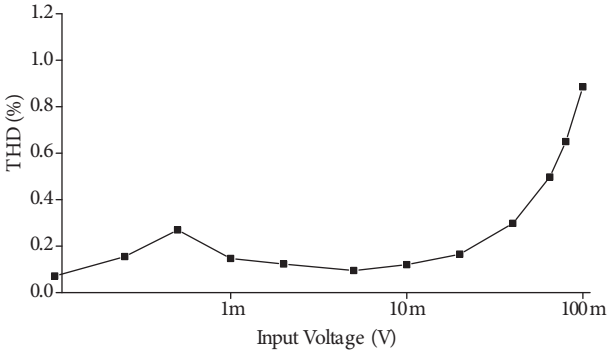

Figure 10. THD against the peak value of the applied sinusoidal signal for the proposed APF.

The total power dissipation of the proposed circuit is approximately 20.6 mW in SPICE simulations. Moreover, the CMOS-based first-order APF circuits in the literature and the proposed one are compared in Table 2: the proposed APF has high input impedance and tunability, and a low number of active and passive

elements. As an example, when compared with the filter configuration in [7] employing five NMOS transistors, the circuit of the present work consists of only three NMOS transistors. Nonetheless, the circuit of the present work has a floating capacitor and does not have low output impedance.

Table 2. A comparison table of MOS transistor-based APF circuits.

References	# of transistors	# of passive passive elements	High Input Impedance	Tunability	Bias requirement(s)	Technology	Power supplies
[**1**]	6	2	No	No	Yes	0.35 μm	3.3 V
[**2**]	9	3	No	Yes	Yes	0.35 μm	$\pm$ 1.5 V
[**3**]	tens	1	Yes	Yes	No	0.25 μm	2.5 V
[**4**]	5	1	No	Yes	No	0.35 μm	$\pm$ 1.5 V
[**5**]	3	3	No	No	Yes	0.35 μm	$\pm$ 1.5 V
[**6**]	2	4	No	No	No	0.18 μm	$\pm$ 0.9 V
[**7**]	5	1	Yes	Yes	No	0.18 μm	$\pm$ 0.9 V
[**8**]	6	1	No	Yes	No	0.18 μm	$\pm$ 0.9 V
This work	3	1	Yes	Yes	No	0.13 mu m	$\pm$ 0.75 V

4. Experimental results

The proposed APF in Figure 1 can be realized by three commercially available discreet NMOS transistors such as 2N7000 for an experimental test. Additionally, to generate control current I_o, a voltage to current converter circuit in Figure 11 employing only one AD844 device, and a resistor, $R = 10\ \mathrm{k}\Omega$, is used. The input voltage of the circuit in Figure 11 is chosen as –1 V. Thus, I_o is obtained as 100 mu A. The passive component C of the experiment test circuit is selected as 1 nF. Furthermore, the DC symmetrical power supply voltages are chosen as $\pm$ 2.5 V. An experimental test is achieved applying a sinusoidal input voltage with a peak to peak amplitude of 200 mV at different frequency values. The gain and phase responses of the experimental test circuit are given in Figure 12. The pole frequency f_o is approximately 86 kHz.

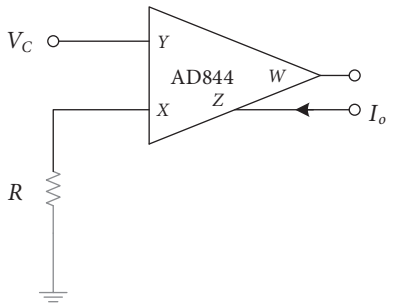

Figure 11. Control current generating circuit.

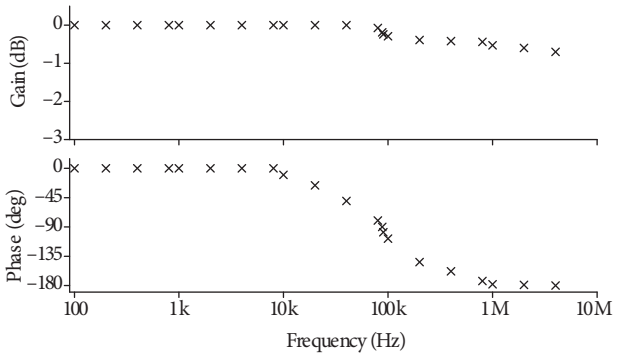

Figure 12. Frequency response of the experimental test circuit.

The simulation and experimental test results confirm the claimed theory well. The difference among ideal, simulation, and experimental results can be attributed to the nonidealities of the NMOS transistors. Moreover, the parasitics of the board affect the performance of the circuit in experimental testing.

5. Conclusion

This paper presents a novel first-order APF employing only three NMOS transistors and a capacitor. The main advantage of the proposed APF is its high input impedance, and thus it can be cascaded with other VM

circuits easily. Its pole frequency can be tuned electronically by a control current. Moreover, it does not require any critical passive component matching conditions and cancellation constraints. It does not have low output impedance and has a floating capacitor. Simulation and experimental test results confirm the theory well, as expected.

References

[1] Maundy BJ, Aronhime P. A novel CMOS first-order all-pass filter. Int J Electron 2002; 89: 739-743.

[2] Metin B, Cicekoglu O. Tunable all-pass filter with a single inverting voltage buffer. In: 2008 Ph.D. Research in Microelectronics and Electronics; 22–25 June 2008; Istanbul, Turkey. New York, NY, USA: IEEE. pp. 261-263.

[3] Olmez S, Cam U. A novel square-root domain realization of first order all-pass filter. Turk J Electr Eng Co 2010; 18: 141-146.

[4] Toker A, Ozoguz S. Tunable allpass filter for low voltage operation. Electron Lett 2003; 39: 175-176.

[5] Yuce E. A novel CMOS-based voltage-mode first-order phase shifter employing a grounded capacitor. Circ Syst Signal Pr 2010; 29: 235-245.

[6] Yuce E, Minaei S. A novel phase shifter using two NMOS transistors and passive elements. Analog Integr Circ S 2010; 62: 77-81.

[7] Minaei S, Yuce E. High input impedance NMOS-based phase shifter with minimum number of passive elements. Circ Syst Signal Pr 2012; 31: 51-60.

[8] Herencsar N, Minaei S, Koton J, Yuce E, Vrba K. New resistorless and electronically tunable realization of dual-output VM all-pass filter using VDIBA. Analog Integr Circ S 2013; 74: 141-154.

[9] Ozoguz S, Abdelrahman TM, Elwakil AS. Novel approximate square-root domain all- pass filter with application to multiphase oscillators. Analog Integr Circ S 2006; 46: 297-301.

[10] Metin B, Pal K. Cascadable allpass filter with a single DO-CCII and a grounded capacitor. Analog Integr Circ S 2009; 61: 259-263.

[11] Metin B, Cicekoglu O. Component reduced all-pass filter with a grounded capacitor and high-impedance input. Int J Electron 2009; 96: 445-455.

[12] Horng JW. High input impedance first-order allpass, highpass and lowpass filters with grounded capacitor using single DVCC. Indian J Eng Mater S 2010; 17: 175-178.

[13] Ibrahim MA, Minaei S, Yuce E. All-pass sections with high gain opportunity. Radioengineering 2011; 20: 3-9.

[14] Yuce E, Pal K, Minaei S. A high input impedance voltage-mode all-pass/notch filter using a single variable gain current conveyor. J Circuit Syst Comp 2008; 17: 827-834.

[15] Pandey N, Paul SK. All-pass filters based on CCII- and CCCII-. Int J Electron 2004; 91: 485-489.

[16] Baker RJ. CMOS Circuit Design, Layout and Simulations. Piscataway, NJ, USA: IEEE Press-Wiley, 2005.

[17] Razavi B. Design of Analog CMOS Integrated Circuits. 1st ed. New York, NY, USA: McGraw Hill, 2001.